SGS-THOMSON MICROELECTRONICS

STA002 CHANNEL DECODER

QPSK DEMODULATOR IMPLEMENTATION NOTE

CONFIDENTIAL

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1. Introduction

The aim of this note is to show the architecture of the QPSK demodulator implemented in the STA002 Channel Decoder. Our attention will be focused on the carrier and timing loops, the schematic and explanation of which are given in the following two chapter.

The next figure shows the overall block diagram of the QPSK demodulator:

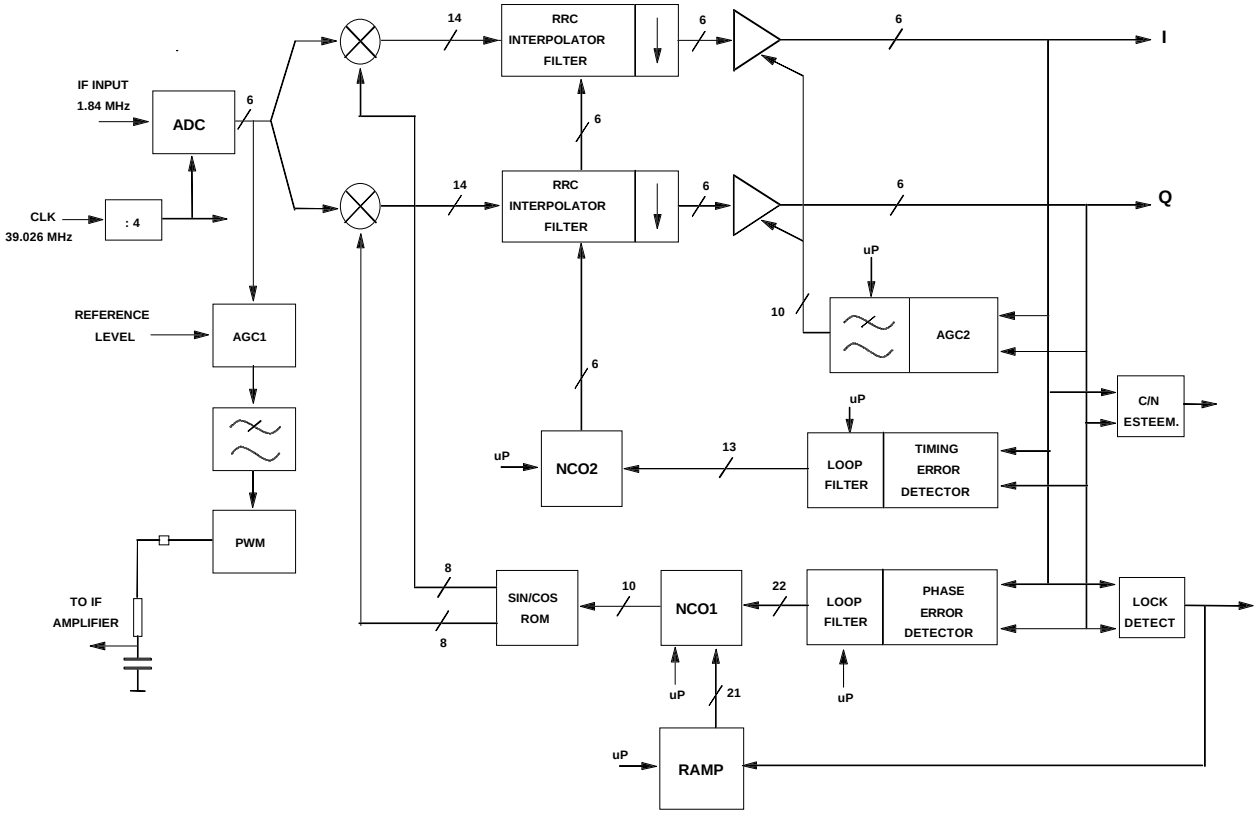

Fig.1 - QPSK demodulator block diagram

The clock reference, coming from the RF front-end unit (STA001), at about 39.02687 MHz is divided by four to get the internal clock at 9.7567 MHz that is used to oversample the 1.84 MHz IF input signal. This signal is quantized on 6 bits and , then, multiplied by the sine an cosine functions to obtain the In-phase and the Quadrature component of the transmitted symbols. After the matched filters (with root raised cosine shape) the two component I and Q of the demodulated QPSK signal are available at the circuit output.

Two Automatic Gain Controls are realized inside the block. The first one (AGC1) is used to keep the input signal at a constant level to avoid the saturation of the A/D converter in presence of noise.
Depending on the bandwidth of the SAW filter used at the first IF, a co-channel interferent signal might increase the input signal power. The AGC1 is not able to discriminate between this signal and the useful one; in this case the second AGC (AGC2) is used for power optimization in the signal bandwidth.
A C/N estimator, a lock detector and an acquisition aiding ramp are also implemented.

2. Carrier Loop

The carrier loop, depicted in fig.2, implements the well known polarity-type Costas loop algorithm operating at symbol frequency.
The input of the carrier loop is the demodulated complex signal. In general this signal is affected by the phase and frequency error that are fixed by the mean of the following devices:

a) a phase error detector;
b) a programmable loop filter;
c) a sine/cosine Digitally Controlled Oscillator (DCO);
e) a quadrature demodulator.

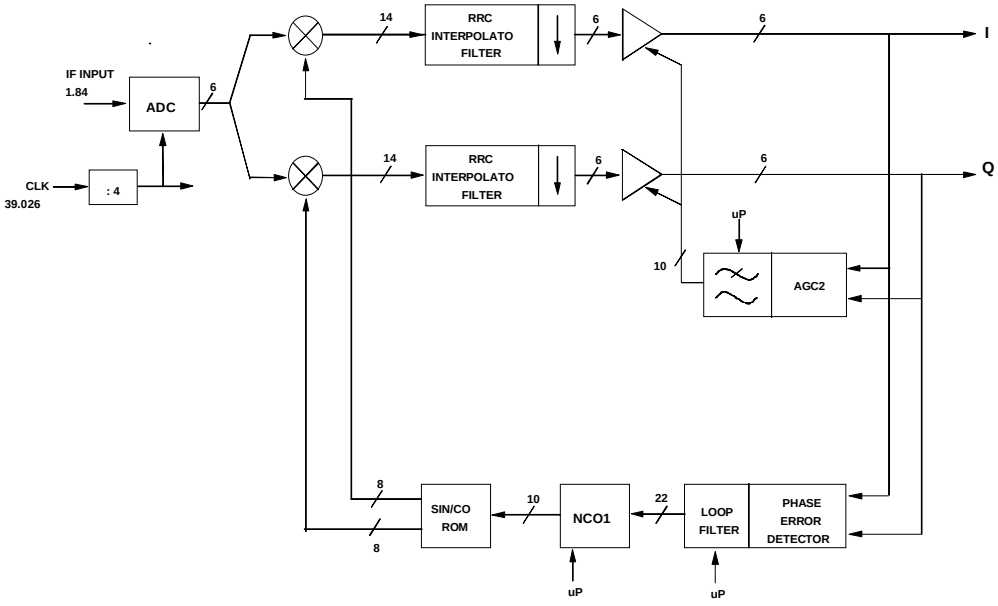

Fig.2 - Carrier Loop

Phase Error Detector
The phase error detector measures the error between the sampled symbols and the quadrant bisector. The circuit adopted is a modification of the polarity-type phase error detector as proposed in [1].
In fig.3.a is shown the schematic of the circuit. Inside the dashed line is the classical phase detector the output of which is given by the following formula (computed at symbol rate):

$$err = I\ sgn(Q) - Q\ sgn(I)$$

This signal is passed to the output (pfdout) only when the demodulated symbol lies outside the region depicted in fig.3.b; in fact, in this case, the flip-flop is enabled by the control logic. When the symbol is inside this region, the circuit holds the previous output of the phase detector so a dc component proportional to the input frequency offset arises. In the steady state, when the loop is locked (and, therefore, the phase error is small), the circuit behaves like a phase detector (PD) while during the acquisition phase it behaves like a phase and frequency detector (PFD). In this way an improvement of the acquisition performance is obtained with no penalty in steady state jitter.

The PFD threshold (PFDTHR) is controlled by an I2C-bus programmable register. For a null value written in the PFDTHR register the circuit becomes a PD both in the acquisition phase and the steady state.

As mentioned in the STA002 Data Sheet [3], the PFDTHR depends on the AGC2_REF parameter and a good value (computed by simulation) is about 0.4*AGC2_REF.

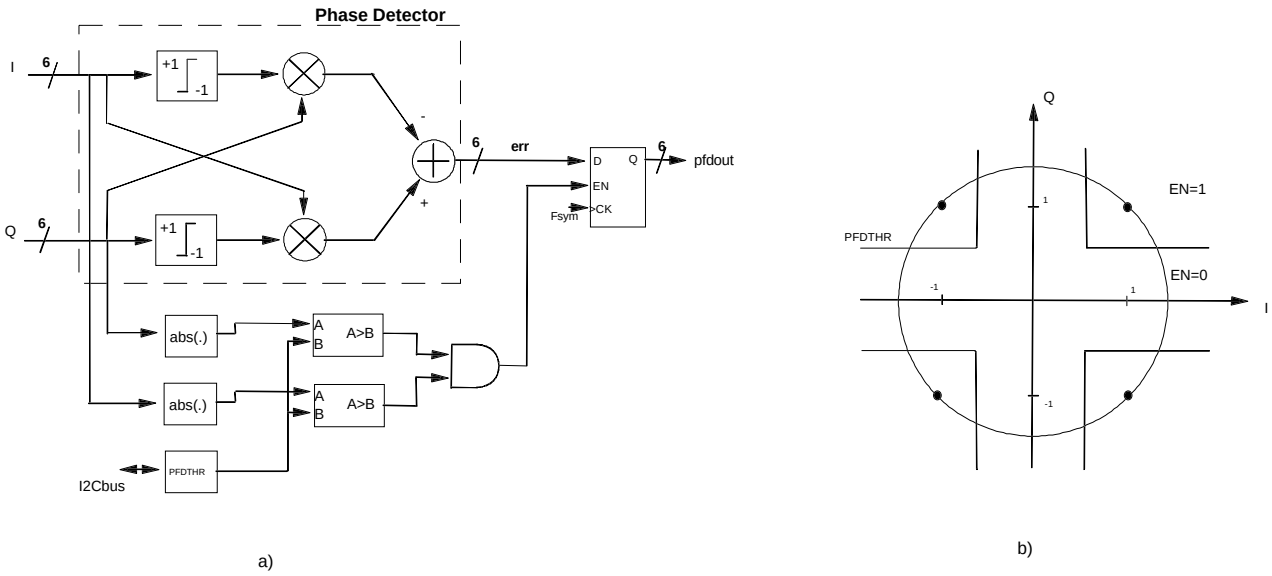

Fig.3 - Phase and Frequency Detector

Loop Filter

The loop filter is a first order IIR with two programmable parameters: one for the proportional correction, the other for the integral correction.

Fig.4 shows the structure of the filter.

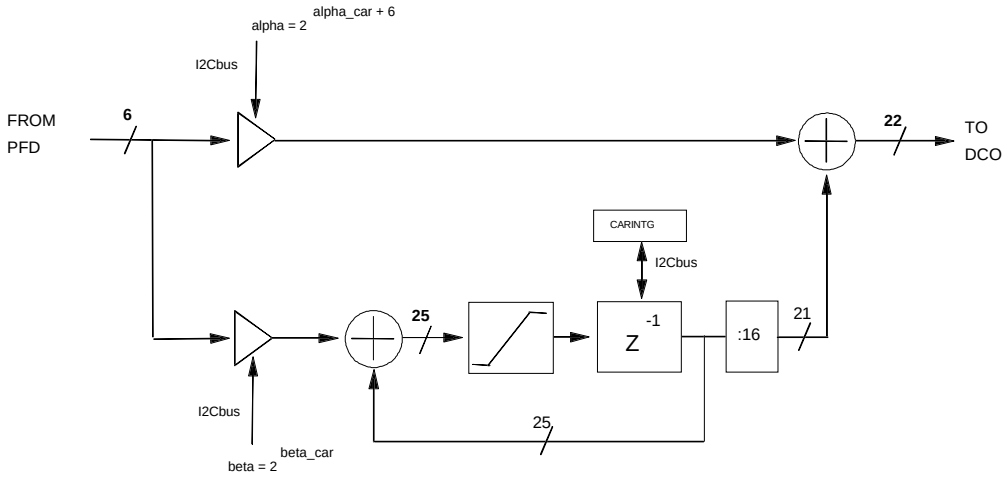

Fig.4 - Carrier Loop Filter

The proportional gain alpha and the integral gain beta of the filter are programmable by the parameters alpha_car and beta_car respectively. The loop natural frequency f_n and the damping factor ξ depend on these two parameters as pointed out in the STA002 data sheet (see para.3.4.2 in [3]).

Digitally Controlled Oscillator (DCO)
The two blocks NCO1 and SIN/COS ROM in fig.2 form the DCO showed in fig.5.
The DCO acts as a quadrature local oscillator to digitally demodulate the IF input signal.

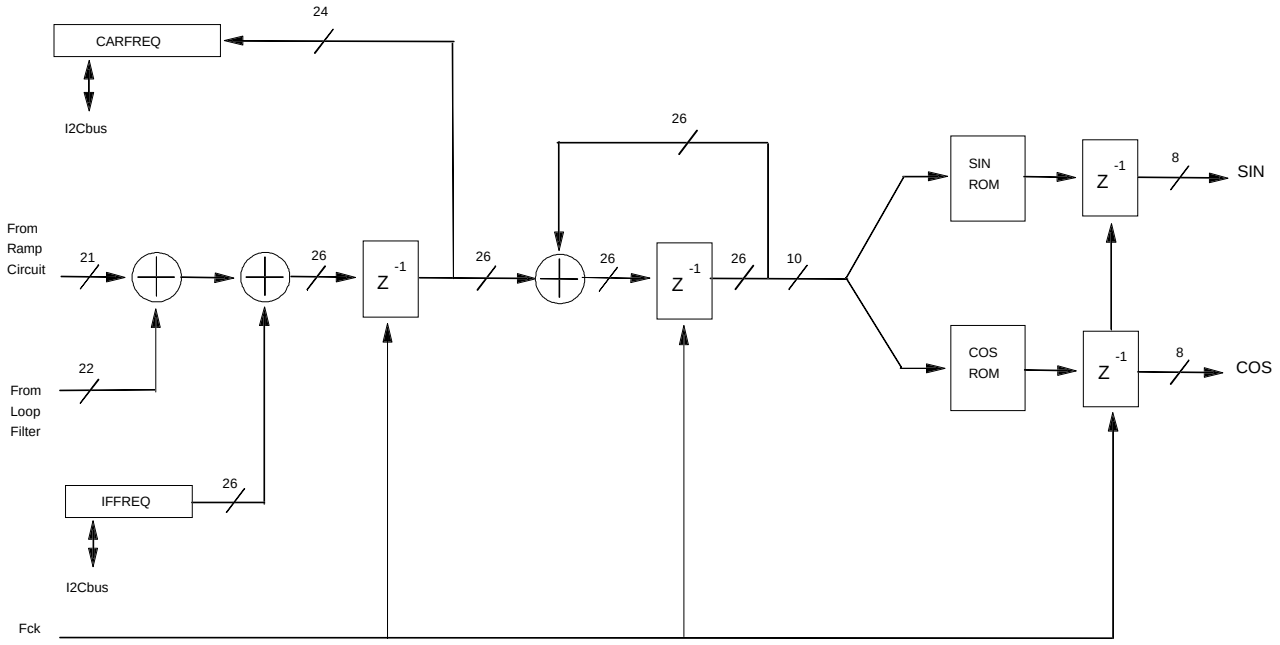

Fig.5 - Digitally Controlled Oscillator

The phase accumulator produces a digital ramp with a resolution of $2\pi/2^{26}$ radians. This signal is frequency modulated by the output of the loop filter. The 10 MSB of the phase register are connected to the address bus of the two look-up tables to produce the digital sine and cosine functions with 8 bits of quantization.

The central frequency f_0 of the oscillator can be programmed via I2C-bus by the IFFREQ register. The output frequency is corrected by the filtered phase error in order to maintain the loop locked.

The sine and cosine output frequency is given by:

$$f_0 = \left(IFFREQ + RAMP + \bar{\varepsilon} \right) \frac{f_{ck}}{2^{26}}$$

where $\frac{f_{ck}}{2^{26}}$ is the DCO frequency resolution (f_{ck} = 9.7567 MHz), IFFREQ is the number programmed in the IFFREQ register in order to tune the DCO at its nominal frequency (namely 1.84 MHz), RAMP is the signal coming from the ramp circuit (this signal is zero if the ramp is switched off) and $\bar{\varepsilon}$ is the filtered instantaneous phase error.

The actual frequency offset between the incoming signal and the local oscillator can be read at any time by the CARFREQ register.

Quadrature Demodulator
The quadrature demodulator is realized by the two input multiplier (fig.2). It simply shifts the spectrum of the IF input signal to the base-band. The two outputs of the quadrature demodulator are connected to the raised root cosine filters that are part of the carrier and timing loops.

3. Timing Loop

The timing loop, depicted in fig.6, is completly implemented digitally. It uses two interpolator filters (one for each component), a timing error detector, a loop filter and a timing generator (NCO2). This loop operates with one sample per symbol. To correct the timing error, at each symbol time, the impulse response of the interpolator filter is shifted by an amount depending on the phase accumulated in the timing generator. Only the central sample of the symbol is output from the timing loop.

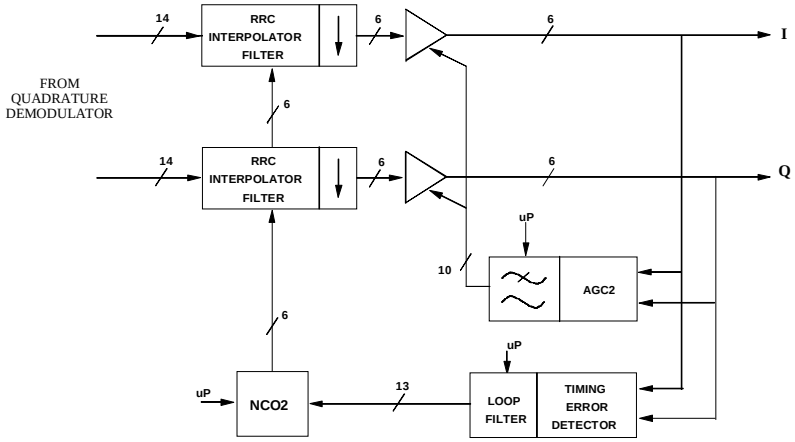

Fig.6 - Timing Loop

Timing Error Detector

The timing detector uses the Mueller&Muller algorithm [2] which works with only one sample per symbol.
The timing error is given by the formula:

$$\varepsilon = I_n \, \mathrm{sign}(I_{n-1}) - \mathrm{sign}(I_n) \, I_{n-1} + Q_n \, \mathrm{sign}(Q_{n-1}) - \mathrm{sign}(Q_n) \, Q_{n-1}$$

This error is controlled by the loop filter by the two programmable parameter alpha_tmg and beta_tmg.

Loop Filter

The structure of the timing loop filter is the same as the carrier loop filter. Fig.7 shows the schematic diagram of the filter.

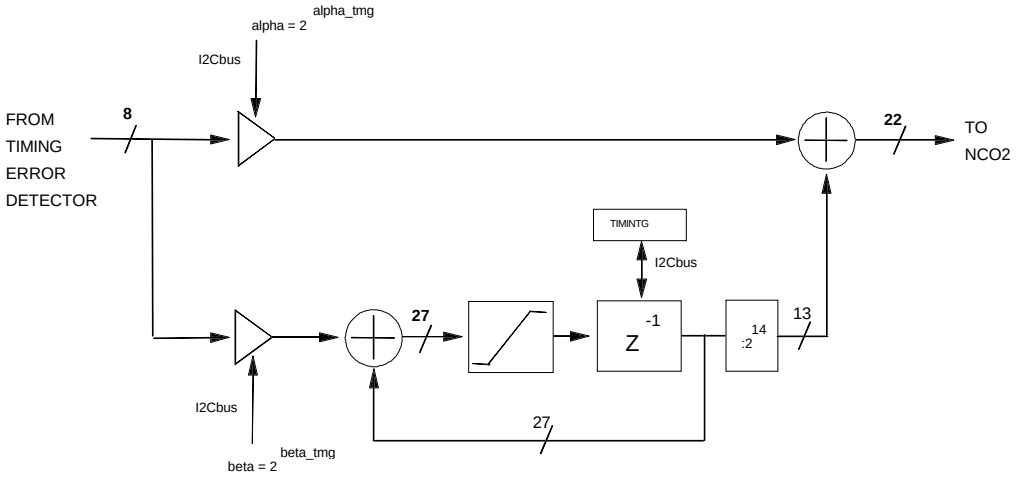

Fig.7 - Timing Loop Filter

Also for this filter the two programmable parameters alpha_tmg and beta_tmg are available to establish the proportional and the integral gain of the loop. The filter output controls the timing generator device.

Timing Generator

The timing generator gives the exact positions of the input samples refered to a virtual symbol clock.
This is done using the accumulator modulo 1 showed in fig.8. At each sampling period the value γ=Fs/Fck is added in the timing register (Fs=symbol frequency=1.84MHz; Fck=clock frequency=9.7567MHz).

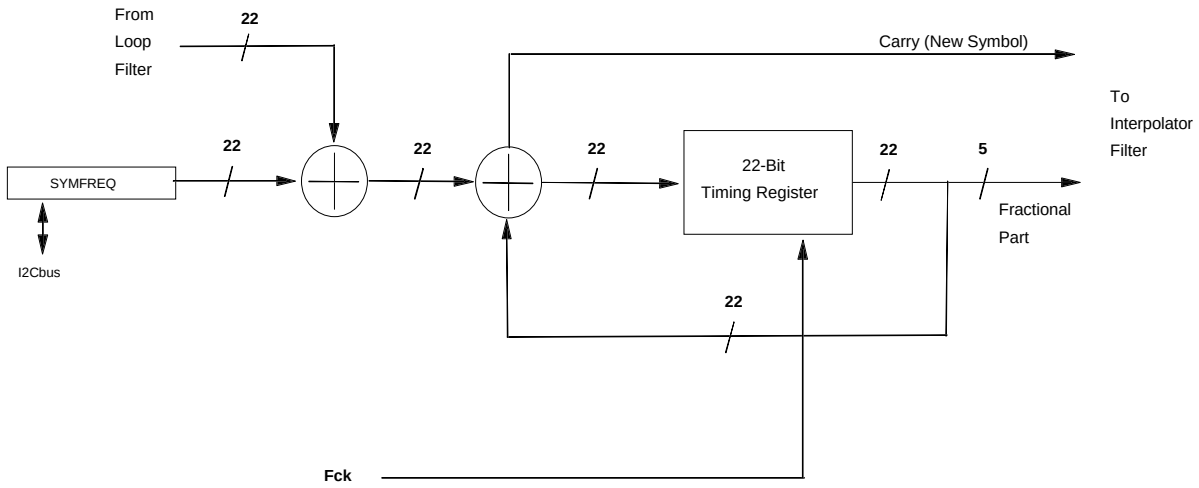

Fig.8 - Timing Generator (NCO2)

Each time the accumulator overflows a new symbol is output. γ<1 is the relative (respect to the symbol period) sampling period. The content of the accumulator gives the fractional part of the timing, i.e. the fraction of the symbol period between the symbol time and the sampling time. In different words, the content of the accumulator delivers the fractional part of the sampling clock which is used by the interpolator filter to choose the coefficient of the impulse response. It plays the role of the timing VCO.
The nominal symbol frequency is programmed by the software writing the SYMFREQ register; an adjustment is provided by the timing loop to find the optimal symbol phase and to correct residual frequency offset.
The actual frequency is:

$$f_0 = \left(SYMFREQ + \bar{\varepsilon}\right) \frac{f_{ck}}{2^{22}}$$

or equivalently

$$f_0 = f_{ck}\ \gamma + \bar{\varepsilon}\ f_s = f_{ck}\ \gamma\ \left(1 + \bar{\varepsilon}\right)$$

where $\bar{\varepsilon}$ is the filtered timing error.

Interpolator and Nyquist Filter

This is used to filter the digital flow and interpolate the value at exact symbol time. The filter output is a succession of symbol values with an average period equal to the nominal symbol period. The filter works both as interpolator and Nyquist filter. In fact, instead of taking any low pass filter, for the interpolation purpose, we use the Nyquist shape (root raised cosine) needed anyway.

The filter has a polyphase structure and is 12 taps long with 32 coefficients per tap i.e. each taps is divided in 32 time interval. The roll-off factor is 0.4.

Bibliography

[1] "New Phase and Frequency Detectors for Carrier Recovery in PSK and QAM Systems",
H.Sari, S.Moridi, IEEE Transactions on Communications, Vol.36, NO.9, Sept. 1988

[2] "Timing Recovery in Digital Synchronous Data Receivers",
K.H.Mueller, M.Muller, IEEE Transactions on Communications, VOL.COM-24, NO.5. May 1976

[3] STA002 STARMAN CHANNEL DECODER Target Specification, Sept. 1997
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