Dielectric breakdown in electrically stressed thin films of thermal SiO_2

Eli Harari

Newport Beach Research Center, Hughes Aircraft Company, Newport Beach, California 92663
(Received 8 August 1977; accepted for publication 8 November 1977)

A novel technique is described which was used to study the intrinsic breakdown mechanism in films of thermal SiO_2 in the thickness range 30–300 Å. It was determined that high-field and high electron injection current conditions existing in the films just prior to breakdown result in the generation of a very high density of defects which behave electrically as stable electron traps. These traps are most likely generated close to the injecting electrode. The internal field in the oxide due to trapped electrons can approach 3×10^7 V/cm which appears to be the maximum field strength which Si-O bonding can withstand. At all temperatures between 77 and 393°K, the breakdown mechanism is intimately related to the rate of generation of the electron traps. No evidence was found to support the impact ionization breakdown model. The technique is also described as a tool for yield measurements, with important implications for long-term reliability of MOS IC's.

PACS numbers: 77.50.+p, 73.60.Hy, 73.40.Qv, 72.20.Ht

I. INTRODUCTION

The rapid development of MOS technology has spurred a considerable interest in the dielectric instabilities in electrically stressed thin films of thermally grown SiO_2. This is a major reliability problem in MOS LSI and will become one of the limiting factors for maximum chip size in high-density high-performance short-channel MOS VLSI.

The majority of related work reported in the past few years[1] has dealt with large-area effects primarily related to pinholes and weak oxide spots. Because breakdown occurs first in these localized regions, their occurrence obscures phenomena associated with the intrinsic oxide breakdown mechanism. Previous researchers have, in general, relied on a self-healing breakdown technique[2–5] to isolate the intrinsic oxide breakdown from early breakdown events. The present paper describes a new technique which was used with considerable success to gain a clearer understanding of the mechanisms related to intrinsic oxide breakdown. The distinguishing feature of this new technique is that the oxide is stressed under a condition of constant oxide current, rather than constant or ramped gate voltage. This ensures a constant electric field at the charge-injecting electrode, independent of charge trapping which may occur in the oxide under the high-field conditions prevailing just prior to breakdown. Measurements were carried out on a very large number of oxide capacitors (more than 10 000 samples from many wafer lots), to ensure valid statistical data and to isolate unusual events. The effective oxide area under stress was kept very small, thereby almost completely eliminating the probability for the occurrence of early breakdowns through pinholes and other localized oxide imperfections. Oxide thicknesses examined were limited to the 30—300-Å range.

A model is proposed which qualitatively describes the mechanisms leading to intrinsic oxide breakdown. The model suggests that breakdown is closely related to the observed generation of a very high density of defects in the stressed oxide. These defects act as efficient and stable electron traps. No evidence was found to support the impact-ionization breakdown model.[6,7]

II. DEFINITION OF TERMS

Three basic parameters are used in the present study to characterize the oxide films. Each thin-oxide capacitor was stressed at a gate voltage so as to maintain a specified oxide current I. $V_{in}(I)$ is the voltage required initially on the gate to achieve an oxide current I. Under continuous electrical stress, charge is trapped in the oxide, necessitating a change in $V_{in}(I)$ in order to maintain I. $\Delta V_{BD}(I)$ is the measured change in gate voltage just prior to breakdown, i.e., $V_{BD}(I)=V_{final}(I)-V_{in}(I)$. Its magnitude is proportional to the density and spatial distribution of the charge trapped in the oxide, its sign being negative for net trapping of holes and positive for net trapping of electrons. $T_{BD}(I)$ is the measured time to breakdown at the constant current I. $+I$ denotes injection of electrons from the Si substrate into the oxide, while $-I$ denotes injection of electrons from the polysilicon gate electrode into the oxide.

III. EXPERIMENTAL PROCEDURE

A schematic of the automated test station used for data collection in these experiments is shown in Fig. 1. An HP 9830A desk calculator was programmed to control the electrical measurements, record the data, and perform statistical analysis. A digitally controlled power supply provided a prescribed constant oxide current I. The voltage required to maintain this conduction current was monitored on a DVM with a high-input-impedance op-amp buffer. The HP 9830A controlled an Electroglas semiautomatic wafer probe station, and each experiment typically involved breakdown measurements of 100—120 capacitors across the entire area of a 2-in. wafer. For each such measurement, probe contact was made with the probe at zero voltage relative to the substrate. The power supply was then ramped at a rate of 2 V/msec up to the voltage $V_{in}(I)$. With a constant current I now flowing through the oxide, the voltage was sampled at 80-msec intervals, compared with

 0021-8979/78/4904-2478$01.10

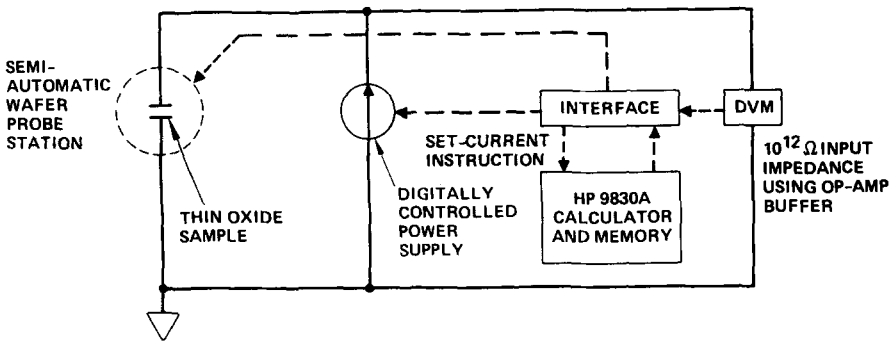

FIG. 1. Automated experimental setup. The required current level is set into the program. The computer prints out and stores the following data: (1) V_{in} (V) at set current, (2) T_{BD} (sec) at set current, (3) ΔV_{BD} (V) at set current.

the previous sampled voltage value, and adjusted, if necessary, to maintain the current constant. Breakdown was arbitrarily determined to have occurred if the last voltage had changed by more than 5% relative to the preceding voltage. Since typical breakdowns result in a sharp voltage drop at the constant current level, the criterion chosen was found to be very effective in determining breakdown to within an 80-msec time interval. When breakdown was established, the calculator recorded I, $V_{in}(I)$, $T_{BD}(I)$, and $\Delta V_{BD}(I)$. A typical set of histograms taken from one wafer is shown in Figs. 2(a)–2(c). The program can interrupt the stress at any specified time prior to $T_{BD}(I)$ and print out the corresponding $\Delta V(I)$, so that the rate at which this parameter is changing with time can be measured, giving information on the gradual buildup of internal fields in the oxide. The program can also isolate those devices which are shorted initially or those rarer "slow" breakdowns where the oxide is very leaky yet not shorted outright.

Other features of the calculator control make is possible to apply the oxide stress in pulses of positive or negative constant current with a predetermined duty cycle or to apply pulses with alternating polarity. Measurements using these techniques can provide information on relaxation and heating effects, mobile ion effects, and the dynamics of trap formation and distribution in the oxide.

The very narrow distributions seen in Figs. 2(a)–2(c) were repeated on almost all batches of the more than 20 separate wafer lots tested. Any of the distributions shown in Figs. 2(a)–2(c) could be repeated to within a few percent on any wafer in the same wafer lot. In Fig. 2(a), the standard deviation for $V_{in}(I) = 8.57$ V is less than 0.10 V over the entire 2-in wafer, indicating uniformity of oxide thickness ($t = 45$ Å) to better than 0.5 Å. Note that this is a far more sensitive thickness uniformity measurement than ellipsometry where the uncertainty in thickness is approximately 5 Å. The sharp $T_{BD}(I)$ distribution is due not only to the very-well-controlled wafer processing, but mainly to the constant current constraint which ensures that slight variations in oxide thickness or internal fields are compensated for externally by the applied $V_{in}(I)$. As will be shown below, $T_{BD}(I)$ has a very strong dependence on the magnitude of I. By way of comparison, we show in Fig. 3 some measurements taken on similar samples where the oxide was highly stressed at a constant applied voltage, allowing the oxide current to decrease with time. The time to breakdown here has a very wide spread, as observed by other workers.[1,8,9]

A second important feature of the experiments is that the area of stressed oxide was kept very small so as to minimize the probability of occurrence of pinholes. Because of the polysilicon gate material and the constant current constraint, self-healing mechanisms cannot be relied upon to neutralize pinhole or weak-spot breakdowns. The effect of oxide area can be seen from the data of Fig. 4, taken under conditions of constant current density. This data represents the distributions of times to breakdown for two capacitor batches on the same wafer, the difference being in the area of stressed oxide. The oxide current density for both groups of capacitors was held at the same value during the measurements. The capacitors were designed so that although one group has an area approximately six times that of the other, both have approximately the same perimeter length. A separate experiment established that the perimeter along the thin-oxide—thick-oxide boundary does not significantly contribute to the thin-oxide current. What is seen from Fig. 4 is that under these identical stress conditions the majority of larger-area capacitors break down within the first 30 sec of stress, while the smaller-area capacitors have a time-to-breakdown distribution which is shifted to much longer times, with the majority of capacitors not breaking down after 300 sec of stress. By further reducing the area, it is possible to almost completely eliminate the early breakdowns, and the resulting time-to-breakdown distribution becomes very sharp, as in Fig. 2(b), representing the intrinsic breakdown phenomena rather than the localized breakdowns due to randomly distributed pinholes and other oxide defects. The area of thin oxide for the capacitors in all the experiments described below was approximately 2.3×10^{-6} cm^2, corresponding to the area of a typical MOS gate in present technology. The thin-oxide area was surrounded at its perimeter by thick thermal oxide, with the gate terminated over this oxide as shown in Fig. 4. ⟨100⟩ Si was used throughout, doped either N^-, P^-, N^+, or P^+. There was no significant difference in oxide breakdown for the substrate doping range 10^{15}–10^{19} cm^{-3}. The gate material was N^+-doped polysilicon. Oxidation conditions were varied using wet and dry oxygen ambients in the temperature range 600–1000°C. Wet oxidations generally were taken through a subsequent N_2 anneal cycle. Samples from each wafer were taken through a 250°C-bias-temperature test and showed no measurable mobile ion contamination.

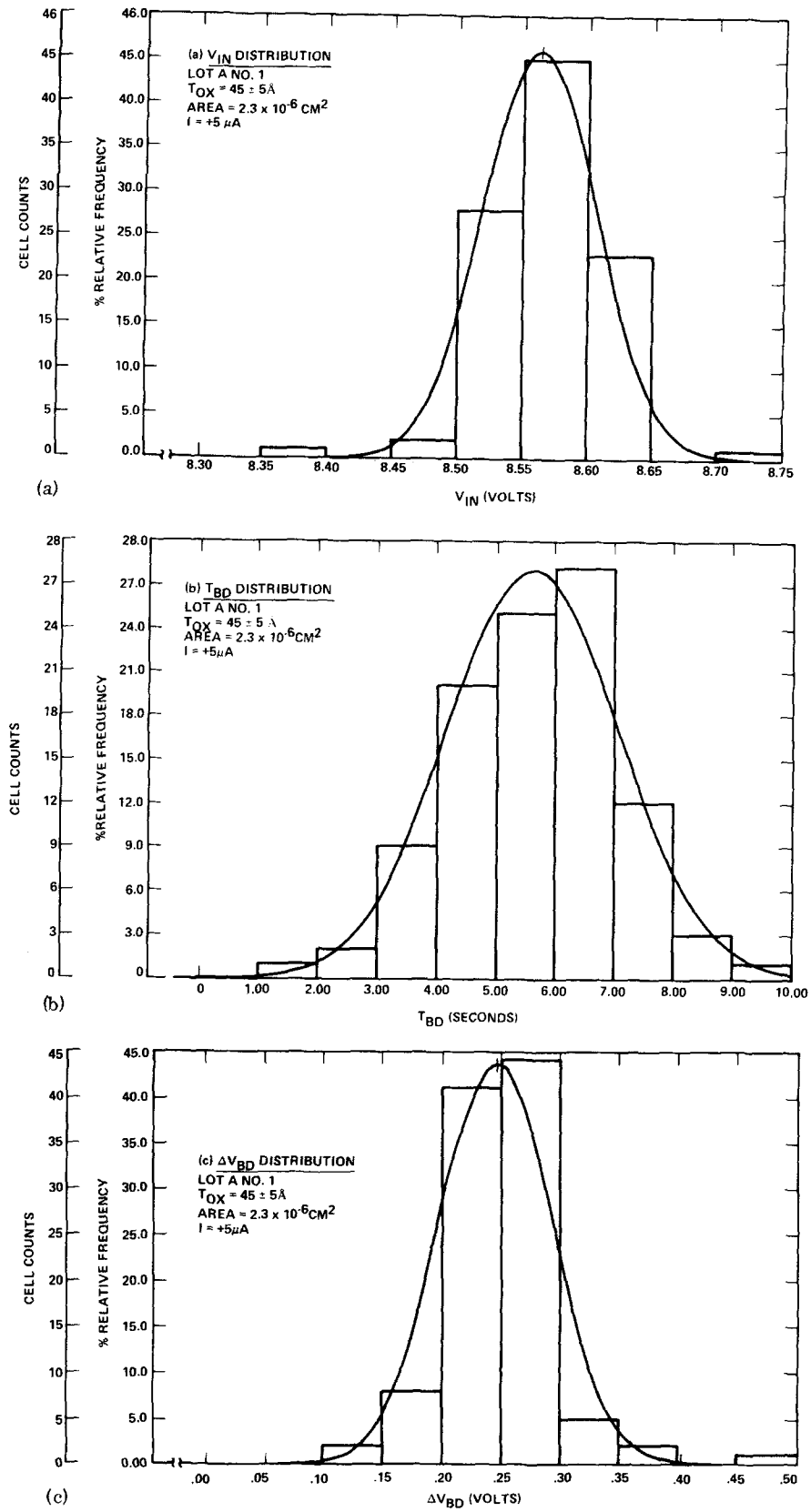

FIG. 2. Typical breakdown data input for a batch of 100 thin-oxide samples: (a) V_{in} distribution, (b) T_{BD} distribution, (c) ΔV_{BD} distribution.

IV. BACKGROUND

Previous workers investigating dielectric breakdown in thin films of thermal SiO_2 have found[1–10] that there are numerous parameters which can affect the outcome of their measurements. Oxide breakdown is affected to a varying degree by oxidation and anneal conditions, oxide fixed charge and charge due to contamination, substrate crystallographic orientation, substrate doping type and level, surface particulates and impurity pre-

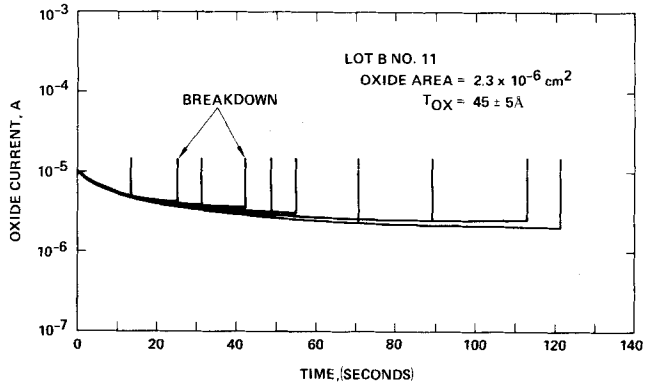

FIG. 3. Measured time to breakdown for thin-oxide samples stressed at a constant gate voltage. T_{BD} at constant V_g.

cipitates, crystallographic imperfections in the substrate close to the surface, type of gate material used, and incorporation of atoms from the gate into the oxide during sintering. Because pinholes and weak oxide spots directly affect yield, most of the previous work has concentrated on deriving processing conditions which would minimize their density. What was not generally appreciated until recently[11] is that even oxides apparently free of pinholes will, under prolonged electrical stress, eventually exhibit destructive breakdown. This is an important aspect in determining long-term reliability.

The experiments described in this paper relate almost exclusively to this intrinsic oxide breakdown. Although intrinsic breakdown, when it occurs, is a localized phenomena, the degradation with time before breakdown occurs uniformly over the entire area of stressed oxide.

The work reported here was prompted by and is closely related to findings from previous work reported recently by the author.[12] That work, conducted on samples similar to those used in the present work, showed that thin films of thermal SiO_2, when stressed at high fields close to breakdown, show a marked buildup of negative charge residing in stable electron traps deep in the oxide forbidden gap. Furthermore, these traps, whose density approaches 1×10^{19} cm^{-3},[12,13] do not exist in the oxide prior to voltage stressing but require high-field conditions for their generation. The maximum breakdown strength of thin films was found to increase with decreasing thickness, in agreement with earlier work,[3,12] approaching an upper limit of approximately 30 MV/cm, as shown in Fig. 5. Before breakdown, the highly stressed oxide can conduct a current density of several A/cm^2 by Fowler-Nordheim tunneling.[14] The work described here characterizes these deep-level electron traps and shows that their generation is intimately related to the oxide breakdown mechanisms.

V. EXPERIMENTAL RESULTS

A. Measurements at constant oxide current

All measurements for a wide range of oxide currents showed a strong correlation between the mean $\overline{T_{BD}(I)}$ and the corresponding mean $\overline{\Delta V_{BD}(I)}$. For oxides of thickness below 100 Å, there was a very strong dependence on oxide thickness for the parameters $\overline{T_{BD}(I)}$ and $\overline{\Delta V_{BD}(I)}$. These parameters were far less dependent on oxidation conditions (wet or dry O_2, with or without nitrogen or argon anneals) and are, therefore, not described separately for each lot. The oxide thickness dependence of $\overline{T_{BD}(I)}$ and $\overline{\Delta V_{BD}(I)}$ is shown in Fig. 6 for $I=+10$ μA. For the very thin films at 33 Å, $\overline{\Delta V_{BD}}$ is close to zero because most injected charge is within direct tunneling distance out of the oxide and will, therefore, not remain trapped.

Each batch of capacitors in Fig. 6 has the $\Delta V_{BD}(I)$ distribution exhibited in Fig. 2(c) and the $T_{BD}(I)$ distribution typified in Fig. 2(b). By examining individual samples, it was found that those samples at the low end of the $\Delta V_{BD}(I)$ distribution were exactly those in the low end of the $T_{BD}(I)$ distribution and so on for each range

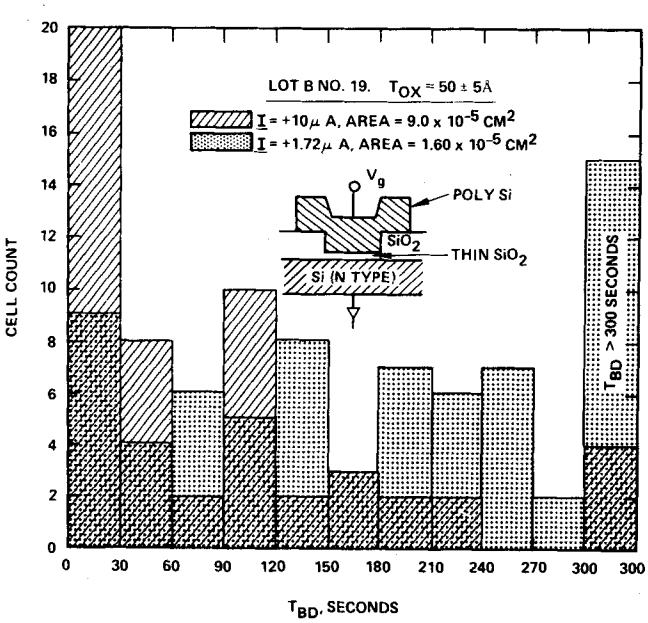

FIG. 4. Effect of area of stressed oxide on the T_{BD} distribution (at constant current density).

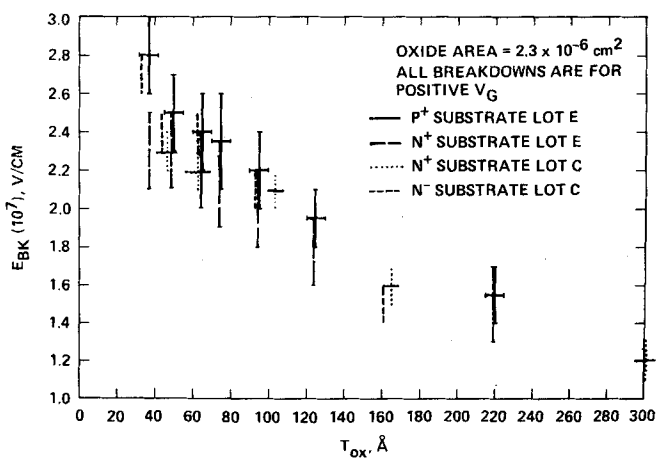

FIG. 5. Oxide breakdown strength for ultrathin oxides as a function of oxide thickness. All data shown for positive V_g. Negative V_g breakdowns are lower by 5—10%.

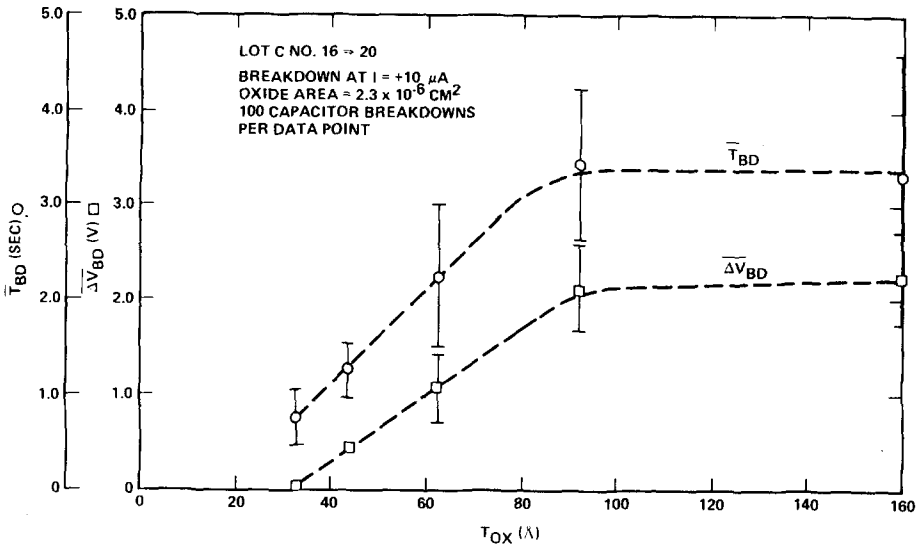

FIG. 6. Effect of oxide thickness on T_{BD} and ΔV_{BD}.

of the distributions. The linearity of this relationship, illustrated in Fig. 7, was obtained for four oxide thicknesses and for up to a factor of 30 variation in the (constant) oxide current. For each current level, the T_{BD} is normalized to the 1-μA current level. That is, it is assumed that an oxide current of, say, 30 μA applied for 1 sec is equivalent to a current of 1 μm applied for 30 sec. This assumption neglects the fact that for a given oxide thickness the field required to achieve the 30-μA oxide current is higher than the field for a 1-μA current. Nevertheless, the relation between $\Delta V_{BD}(I)$ and $T_{BD}(I)$ appears to be remarkably linear and follows the same slope for all samples except for samples from wafer 17, which have an oxide thickness of 44 Å. The discrepancy in the slope for samples from wafer 17 suggests that the electrons giving rise to $\Delta V_{BD}(I)$ are trapped predominantly near the injecting electrode. Only for the 44-Å oxides can these electrons be tunneled directly out of the oxide, giving a smaller net $\Delta V_{BD}(I)$ than observed in the thicker films. The five points in Fig. 7 with negative values of $\Delta V_{BD}(I)$ are probably caused by the outward tunneling of electrons which are trapped initially in the oxide during the device fabrication process.

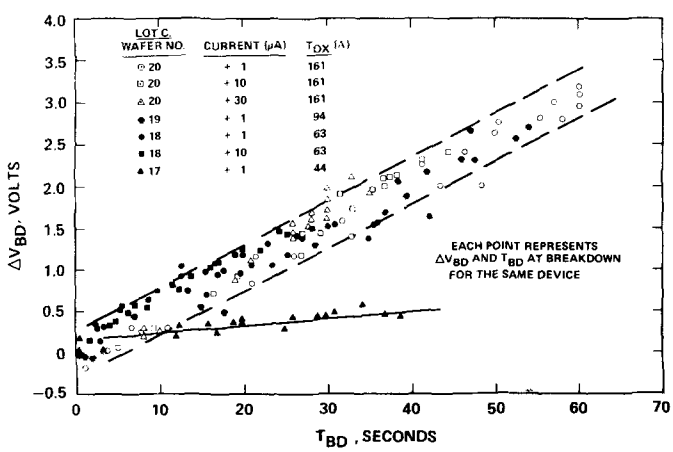

FIG. 7. Relation between ΔV_{BD} and T_{BD} for individual samples of different thicknesses. All T_{BD} values are normalized to a +1-μA current level by assuming $T_{BD}(I)I$ = const.

Although the presence of both a high stress field and an oxide current are necessary to initiate breakdown, the data shown in Fig. 8 suggests that the current density is the more important parameter. Shown in Fig. 8 is the $\overline{T_{BD}(I)}$ values for different constant current levels in the range 1—60 μA. The same data are included in Table I, together with the corresponding values of $V_{in}(I)$. Taking the data for wafers 19 and 20, an increase by a factor of 60 in current, which is accom-

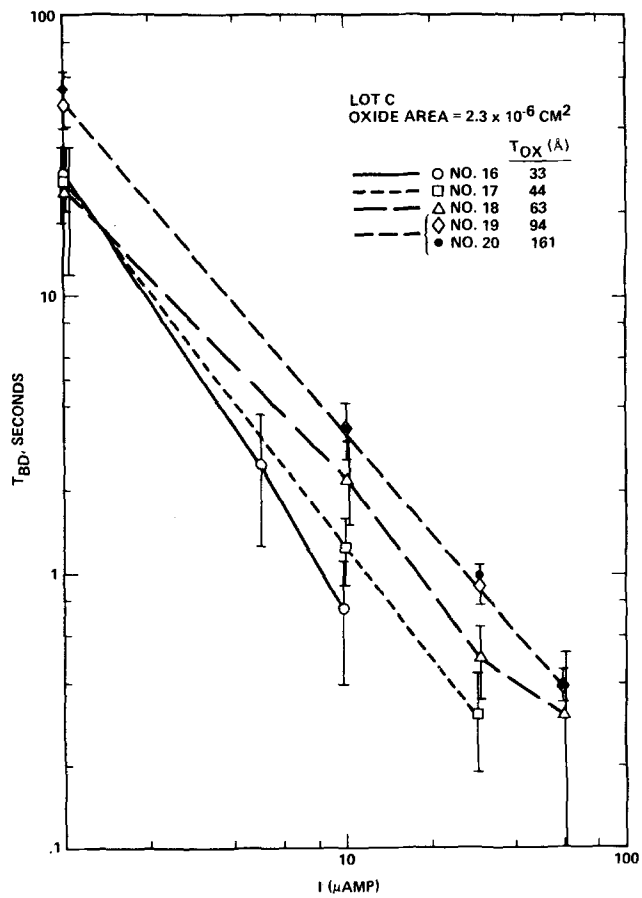

FIG. 8. Relation between $T_{BD}(I)$ and the magnitude of I.

TABLE I. Lot C. T_{BD} at different oxide currents. T_{BD} is given in sec, V_{in} in V.

Wafer No.	Thickness (± 5 Å)	$I=1\ \mu A$		$I=5\ \mu A$		$I=10\ \mu A$		$I=30\ \mu A$		$I=60\ \mu A$	
		T_{BD}	V_{in}	T_{BD}	V_{in}	T_{BD}	V_{in}	T_{BD}	V_{in}	T_{BD}	V_{in}
16	33	27 ± 7	6.77 ± 0.09	2.5 ± 1.25	7.19 ± 0.04	0.74 ± 0.33	7.39 ± 0.04				
17	44	26 ± 8	8.39 ± 0.06	• • •	• • •	1.24 ± 0.32	9.10 ± 0.10	0.31 ± 0.13	9.55 ± 0.03		
18	63	23 ± 11	10.88 ± 0.07	• • •	• • •	2.25 ± 0.75	11.91 ± 0.09	0.50 ± 0.15	12.50 ± 0.08	0.31 ± 0.23	12.92 ± 0.06
19	94	47 ± 8	13.91 ± 0.42	• • •	• • •	3.38 ± 0.78	15.00 ± 0.15	0.92 ± 0.15	15.57 ± 0.13	0.39 ± 0.06	16.01 ± 0.11
20	161	54 ± 8	19.31 ± 0.13	• • •	• • •	3.32 ± 1.24	20.45 ± 0.14	1.0 ± 0.15	21.02 ± 0.15	0.38 ± 0.05	21.43 ± 0.16

panied by an increase by approximately a factor of 0.15 in the field [as shown by $V_{in}(I)$] results in a decrease by approximately a factor of 120 in T_{BD}. The deviation from a one-to-one relationship between $T_{BD}(I)$ and I^{-1} is probably brought about by the small increase in $V_{in}(I)$.

B. Measurements at different duty cycles

Two batches, each with 100 capacitors on the same wafer, were stressed under pulsed current conditions with a different duty cycle for the two groups. The first group was subjected to a succession of pulses of 140-msec duration of -10-μA constant current at a 50% duty cycle. The other had the same -10-μA current pulses but applied at a 2% duty cycle. $T_{BD}(I)$ was measured only during stress time for both cases. The $T_{BD}(I)$ distributions for the two cases are shown in Fig. 9. There is clearly no significant difference. The experiment was repeated also for the opposite (positive) polarity current pulsing with the different duty cycle again showing no significant effect on $T_{BD}(I)$.

This experiment demonstrated that heat generated in the conducting oxide is sufficiently efficiently dissipated in the gate and substrate to have no significant effect on the breakdown mechanism. The experiment also showed that any relaxation effects in the stressed oxide occur, if at all, over a time span much longer than 7 sec, the time between pulses in the 2% duty cycle experiment. We therefore conclude that the high oxide stressing with positive or negative fields has a cumulative effect in bringing the oxide closer to breakdown. Thermal annealing experiments now in progress strongly support this conclusion. This is important for the reliability of devices which during a lifetime of operation may gradually approach the condition for catastrophic breakdown.

C. Low- and High-temperature measurements

Experiments were conducted to measure $T_{BD}(I)$ on identical oxide capacitors stressed at room temperature and at 77°K. Twelve capacitors on a chip were packaged in each 14-pin dip. Six of the 12 were stressed at -1 μA at room temperature, the other 6 were stressed at the same current level with the package immersed in a liquid N_2 bath. $T_{BD}(I)$ and $V_{BD}(I)$ were measured and are shown in Figs. 10 and 11, respectively. From Fig. 10, it is evident that breakdown occurs almost 10 times sooner at room temperature than at 77°K. This finding was confirmed on other samples and also holds true for stressing with the opposite oxide field polarity. On the other hand, the data of Fig. 11 shows that at breakdown $V_{BD}(-1\ \mu A)$ is almost identical at the two temperatures. A correlation of each individual data point in Figs. 10 and 11 can help to explain this apparent discrepancy. By examining each capacitor individually and plotting its $V_{BD}(-1\ \mu A)$ versus $T_{BD}(-1\ \mu A)$ at each temperature, two curves shown in Fig. 12 were obtained. A best fit gives a slope at room temperature which is approximately 10 times the slope at 77 °K. This suggests that under identical oxide stress conditions with identical current density through the oxide generation of traps and trapping of electrons occurs at a much faster rate at room temperature than at 77 °K, and this appears to be the cause for the much faster time to breakdown at room temperature.

Similar results were obtained with batches of capacitors stressed at various temperatures between -150

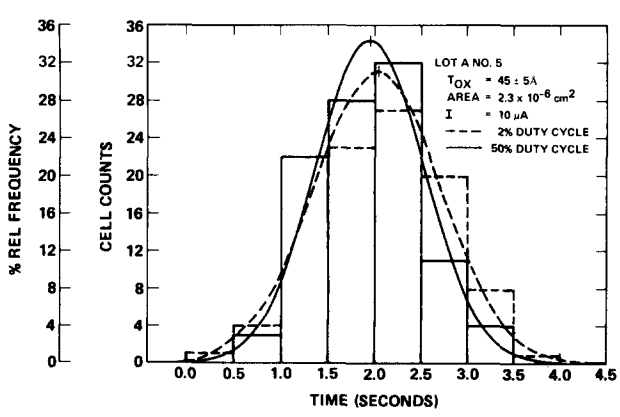

FIG. 9. T_{BD} distributions at 2 and 50% duty cycle constant current pulsing.

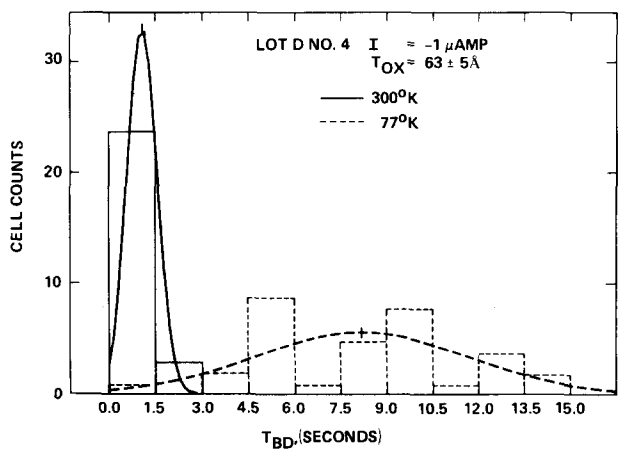

FIG. 10. T_{BD} distributions at 77 and 300 °K with otherwise identical conditions.

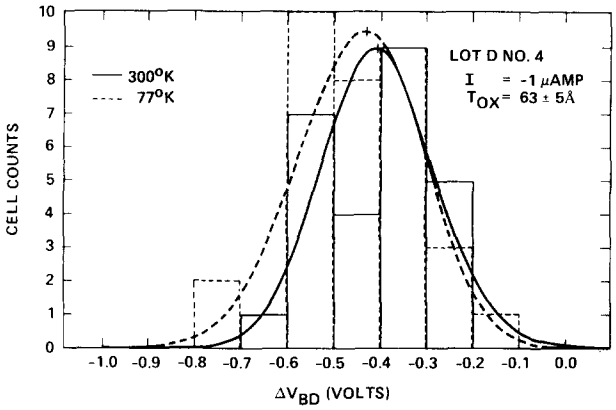

FIG. 11. ΔV_{BD} distributions for the samples of Fig. 10.

and + 120°C on a heat chuck. With these samples, the change in $V_{in}(I)$, $\Delta V(I)$, was plotted continuously with time until breakdown. At any given temperature, all samples from the same batch exhibited identical slopes of $\Delta V(I)$ versus time, independent of their final values of T_{DB}. Typical slopes are shown in Fig. 13 for stress temperatures of −15, +20, +70, and +120°C. The statistical data for these batches (approximately 100 samples in each batch) is given in Table II. We see that the mean $\overline{\Delta V_{BD}}$ is very nearly the same at all four temperatures, while the relative values of $\overline{T_{BD}}$ at each temperature closely follow the corresponding slopes of Fig. 13.

This data has important implications for long-term reliability of IC's operating at high temperatures. It indicates that at higher temperatures the gate oxide is degraded considerably faster due to a very significant increase in the rate of generation of electron traps. Since this is a cumulative effect, even short-term exposures to high temperatures (say, 150–200°C) during operation can result in permanent degradation and weakening of the gate dielectric.

TABLE II. Lot C. Effects of stress temperature.

Temp. (°C)	V_{in} (V)	T_{BD} (sec)	V_{BD} (V)	Slope $V(I)/t$ from Fig. 13 (V/sec)
−15	17.14 ± 0.34	64 ± 5	2.2 ± 0.6	0.020
+20	17.20 ± 0.32	40 ± 5	2.2 ± 0.4	0.053
+70	17.30 ± 0.36	20 ± 3	2.4 ± 0.4	0.100
+120	17.20 ± 0.33	9 ± 2	2.3 ± 0.4	0.200

D. Measurements with alternating field

Constant current stress measurements were performed with alternating pulses of positive and negative gate voltage applied to the thin-oxide capacitors. As with single polarity pulsing, the oxide current during each pulse was kept constant at a predetermined level. The control program was modified so that the magnitude of current and the duration of pulses could be set independently for the positive and negative parts of the cycle. For each sample tested, the output data consisted of $V_{in}(+I_1)$, $V_{in}(-I_2)$, $\Delta V_{BD}(+I_1)$, $\Delta V_{BD}(-I_2)$, and T_{BD}. Here $V_{in}(+I_1)$ is the gate voltage required to initially establish the current $+I_1$ during the first positive pulse, $V_{BD}(+I_1)$ is the change in this voltage required to maintain the current $+I_1$ in the last positive pulse before breakdown, and similarly for $V_{in}(-I_2)$ and $\Delta V_{BD}(-I_2)$ for the negative pulses at current magnitude $-I_2$. T_{BD} is the total time to breakdown, which includes both positive and negative pulses, but excludes the time elapsed between successive pulses.

Alternating polarity measurements can provide information of the dynamics of oxide trap formation and breakdown which dc or pulsed dc measurements do not adequately address. Effects due to mobile ions if present in the oxide are eliminated because under

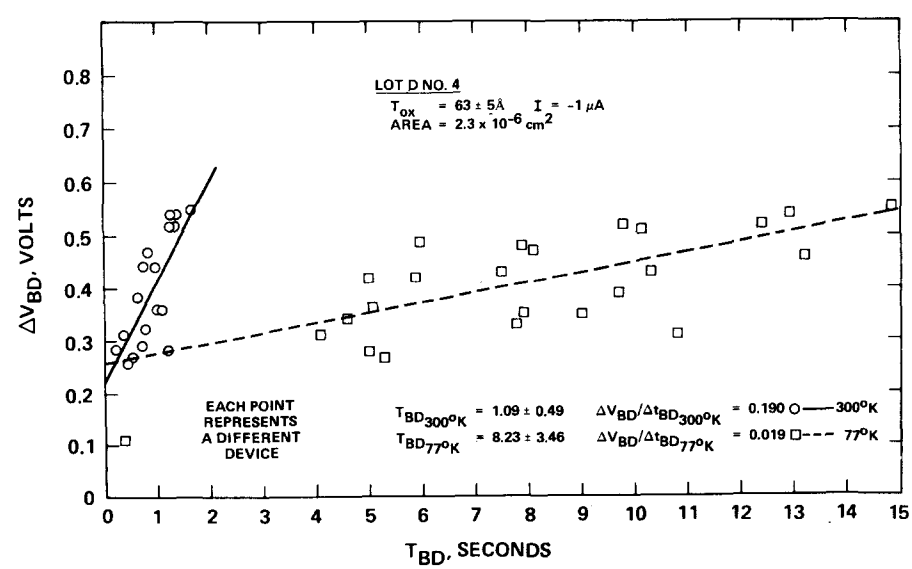

FIG. 12. Relation between ΔV_{BD} and T_{BD} for individual samples stressed under identical conditions at either 77 or 300°K.

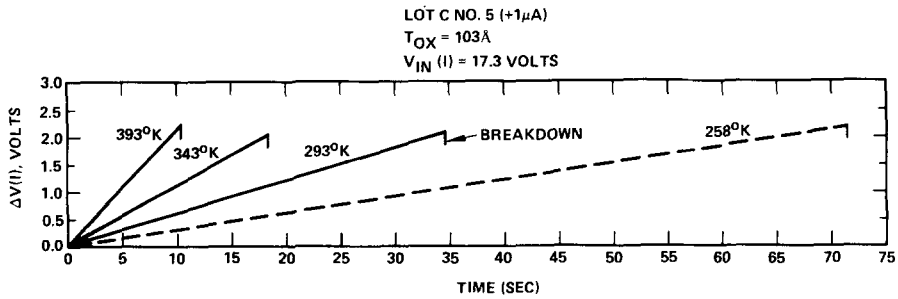

FIG. 13. Change in $V_{in}(I)$ as a function of time under constant current stress at various temperatures.

alternating field stressing there can be no net buildup of mobile ions at one interface. By changing the relative amplitude or pulse duration of either the positive or negative current pulses, it is possible to establish differences, if any, in the relative densities and capture cross sections of the traps associated with breakdown when injection occurs from one rather than the other electrode.

In all the alternate pulsing measurements, the substrate and polysilicon gate were doped N^+ ($\sim 1\times10^{19}$ cm^{-3} phosphorus). Six sets of measurements were performed, each involving a group of approximately 100 capacitors with all six groups from the same wafer. The sequence of pulsings for each measurement is shown in Table III which also contains the mean values of $V_{in}(+I_1)$, $V_{in}(-I_2)$, $\Delta V_{BD}(+I_1)$, $\Delta V_{BD}(-I_2)$, and T_{BD}. The first three experiments have equal duration ($1t = 140$ msec) for both positive and negative pulses. The last three have the same positive pulse duration ($1t$) but different durations for the negative pulses ($4t$, $7t$, and $11t$). These experiments will be discussed in Sec. VI.

E. Yield studies

The automated test system was also used with larger-area oxide capacitors to obtain a comparative measure of oxide integrity as a function of its thickness. The oxide area under stress for each device was 1.8×10^{-4} cm^2, and 120 such devices from across the entire wafer area constituted a sample. Each capacitor was stressed for 2 sec at a constant current level with $V_{in}(I)$ typically less than 15% below the breakdown voltage (obtained from fast ramping to breakdown on several representative capacitors). As with previous measurements, the constant current constraint ensures a good control as well as equal stressing of each device in the sample. A capacitor was assumed to have passed the yield test if $V_{in}(I)$ was within ±5% of the mean $V_{in}(I)$ and if ΔV_{BD} $< |0.5\ V|$ at the end of 2 sec of stressing. This yield criterion eliminates both initial shorts and devices which require the very high stress to either short or to degrade in a manner which would indicate future premature breakdown. This second group is of greater importance for VLSI since the oxide would stand up to normal IC chip testing but would degrade more rapidly than good oxide, causing severe reliability problems after prolonged chip operation. Some of the data obtained with this test is shown in Fig. 14. There are four lots, each with various film thicknesses, with thermally grown wet oxides and dry O_2 oxides. A striking result of these measurements is that there is no reduction in yield for decreasing film thickness down to about 70 Å. This is an encouraging result for VLSI MOS technology, where channel lengths of 1 μm or less require gate oxides of thicknesses of 300 Å or less. The unforgiving nature of the high-field stress test makes it a very powerful tool for quantitatively testing if and how various processing steps can affect the long-term integrity of the gate oxide.

VI. DISCUSSION

The experimental evidence presented above points to a strong correlation between the generation of electron traps under the high stress conditions and the subsequent oxide breakdown. The almost linear relation between $\Delta V_{BD}(I)$ and $T_{BD}(I)$ for all values of $T_{BD}(I)$ in Fig. 7 is the strongest indication for the important role played by the electron traps. We know[12] that these traps do not exist in the oxide before stressing. Furthermore, if the Fowler-Nordheim injection current was merely filling existing electron traps in the oxide, then $\Delta V_{BD}(I)$ would saturate exponentially with time, as is normally observed in photoinjection experiments[15] where filling of a fixed density of traps occurs. The linear time dependence of $\Delta V_{BD}(I)$ observed in Fig. 7 for room temperature and in Figs. 12 and 13 for other temperatures indicates that oxide traps are not merely filled with time, but are also created with time at a uniform rate which holds all the way until breakdown occurs. It stands to reason that breakdown occurs when a cer-

TABLE III. Lot C, $t_{ox} = 103 \pm 5$ Å. I is given in μA, V_{in} and ΔV_{BD} in V, and T_{BD} in sec.

	$+I_1$	$-I_2$	$V_{in}(+I_1)$	$V_{in}(-I_2)$	$\Delta V_{BD}(+I_1)$	$\Delta V_{BD}(-I_2)$	T_{BD}
(a)	+ 10	− 10	+ 18.43 ± 0.34	− 17.38 ± 0.23	+ 1.67 ± 0.41	− 1.33 ± 0.30	7.50 ± 2.50
(b)	+ 1	− 10	+ 17.13 ± 0.30	− 17.07 ± 0.23	+ 0.12 ± 0.12	− 1.49 ± 0.38	4.4 ± 2.0
(c)	+ 10	− 1	+ 18.38 ± 0.29	− 16.15 ± 0.26	+ 1.68 ± 0.29	− 0.18 ± 0.07	4.9 ± 1.0
(d)	+ 10	− 1(4t)	+ 18.28 ± 0.33	− 16.32 ± 0.32	+ 1.26 ± 0.44	− 0.52 ± 0.10	3.9 ± 1.2
(e)	+ 10	− 1(7t)	+ 18.31 ± 0.34	− 16.38 ± 0.33	+ 1.34 ± 0.34	− 0.91 ± 0.15	5.0 ± 1.1
(f)	+ 10	− 1(11t)	+ 18.46 ± 0.26	− 16.52 ± 0.24	+ 1.59 ± 0.48	− 1.93 ± 0.40	6.0 ± 1.3

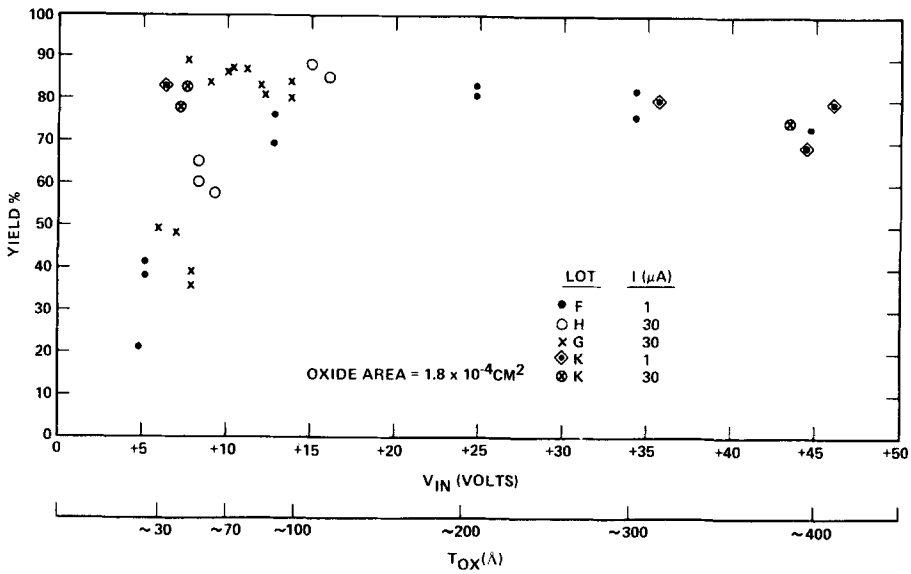

FIG. 14. Yield as a function of oxide thickness for batches of oxide capacitors stressed at constant current.

tain density of electron traps has been exceeded, resulting in localized fields of magnitude higher than approximately 30 MV/cm which, as seen from Fig. 5 is the maximum field at breakdown in the thinnest films (which because of their thinness cannot have any trapped electrons). The linearity of ΔV_{BD} as a function of oxide thickness in Fig. 6 may indicate that initiation of breakdown is localized at the Si-SiO_2 interface. That is, for thicknesses less than 100 Å, the e-traps are located predominantly very near the injecting electrode (as observed independently by Solomon[16]), and their density at breakdown is the same for each of the films. The saturation at ~100 Å implies the existence of a transition region at that thickness and requires further study.

The measurements at different duty cycles indicate that heating or relaxation effects do not contribute to the breakdown mechanism in any significant manner. This is consistent with a constant rate of formation of oxide traps. Relaxation can take place either through annealing of the oxide defects or through emission of trapped electrons. The first is an unlikely possibility because annealing experiments currently in progress indicate no significant anneal in nitrogen ambient below approximately 450°C. Emission of trapped electrons almost certainly occurs in the time intervals between pulsing, but the same values of $T_{BD}(I)$ for the two different duty cycles indicates that the electron traps have such a high capture cross section that they are refilled a very short time after the start of the subsequent current pulse.

The electrical stability of the generated electron traps can be understood in view of the fact that under the high-field conditions to achieve the high Fowler-Nordheim tunneling current any electrons trapped within approximately 4 eV below the oxide conduction band would be within direct tunneling distance (up to ~30 Å) from this energy level. They would, therefore, emit their electrons and not contribute to the value of $\Delta V_{BD}(I)$. In other words, the experimental method would not normally detect the presence of any traps except for those deep stable defects which do not emit their trapped charge. Other experiments such as trap filling followed by photodepopulation[17] should reveal the presence, if any, of shallow traps which, in any case, are less important for breakdown because of their uncharged state. Field emission is believed to be responsible also for the low or zero values of $\Delta V_{BD}(I)$ in films of thicknesses below approximately 40 Å. That is, these films may experience the same generation of deep traps which, however, serve to only momentarily trap injected electrons.

It is well known that hole mobility in SiO_2 has a strong temperature dependence, with holes becoming practically immobile at 77°K.[18–20] If the impact-ionization breakdown model[6,7] holds true, then breakdown under given stress conditions should occur sooner at 77°K than at room temperature. The stressing experiments at 77°K and at higher temperatures up to 393°K show not only that impact ionization cannot be the responsible mechanism for the oxide breakdown (at least for the thickness range below ~160 Å), but also that the breakdown is directly tied to the generated deep electron traps. To begin with, breakdown for any batch and for all temperatures occurred at approximately the same value of $\Delta V_{BD}(I)$ which, by its sign, corresponds to net trapping of electrons, not holes. It may be that the slower increase of ΔV_{BD} at lower temperatures is due to partial compensation from trapped holes, but a more likely explanation is that at lower temperatures injected electrons undergo less electron-phonon interactions, and, therefore, there is a slower rate of generation of defects. Whichever is the case, the fact still remains that when the rate for defect formation is slower, the time to breakdown is also longer by almost the same factor (Table II). Also, since ΔV_{BD} is the same at all temperatures while Na^+ ions are practically immobile at 77°K, the breakdown mechanism here is evidently not affected by any such impurity ions. The impact-ionization model predicts that no holes should be formed in the oxide for a gate voltage below ~12.2 V. Any formation of holes would be experimentally detected in a reduction or saturation in the value of $\Delta V_{BD}(I)$ or in reduction of the rate at which the net negative charge in the oxide increases with time of stress. In Figs. 7,

12, and 13, there is no indication of saturation, and from Table I, T_{BD} (~60 μA) is almost the same for sample number 20 with $V_{in}(60\ \mu A) = 21.43$ V as for sample number 18 with $V_{in}(60\ \mu A) = 12.92$ V, although the former would be expected to show considerably more impact ionization taking place because of the higher potential drop across the oxide. It appears, then, that impact ionization, if it does indeed take place in films of thickness less than 160 Å, does not significantly contribute to the intrinsic breakdown mechanism.

We come now to analyze the data of Table III. In experiment (a), $\Delta V_{BD}(+I_1)$ was different from $\Delta V_{BD}(-I_2)$, which is not surprising since the field at the injecting electrode is sensitive not only to the density of filled electron traps but also to their spatial distribution in the oxide relative to that electrode. Experiment (b), in which $-I_2$ was the same as in experiment (a), gave approximately the same $\Delta V_{BD}(-I_2)$, but $\Delta V_{BD}(+I_1)$ was at least an order of magnitude smaller than for case (a), and this is directly related to the order-of-magnitude reduction in $+I_1$. Similarly, for case (c), where the currents were reversed, $\Delta V_{BD}(+I_1)$ was the same as in case (a), while $\Delta V_{BD}(-I_2)$ was almost an order of magnitude smaller. This suggests that $\Delta V_{BD}(+I_1)$ and $\Delta V_{BD}(-I_2)$ represent different distributions of trapped electrons. This is supported by the T_{BD} data which is approximately the same for cases (b) and (c) but significantly longer for case (a), contrary to what one would expect if a single trap distribution was responsible for both $\Delta V_{BD}(-I_2)$ and $\Delta V_{BD}(+I_1)$. In terms of two distinct trap densities, one at each injecting electrode, the internal localized field in the oxide would be smaller in case (a), where the densities of traps are closely balanced, than in cases (b) or (c), where the density of traps at one electrode would far exceed that at the opposite electrode. There is significance also in the fact that T_{BD} in case (b) is approximately the same as in case (c). This suggests a similar breakdown mechanism for injection from either electrodes despite the fact that the substrate (N^+ crystalline Si) has an interface with a thermally grown oxide, while the gate (N^+ polycrystalline Si) has a deposited interface.

The data in Table III, cases (d)—(f), is more difficult to interpret because T_{BD} includes an increasingly longer pulse at the lower ($-1\ \mu$A) current pulse. Nevertheless, the data is consistent with two separate trap distributions generated at both interfaces during pulsing. Since the filled traps most effective in influencing the value of ΔV_{BD} are close to the injecting electrode, and since these traps are also least likely to lose their charge by field emission, it appears that generation of the deep level of electron traps occurs predominantly at the injecting electrode. It is interesting to note that several other investigators have reported generation of deep electron traps in thermal SiO_2 which has been highly stressed,[21–23] electron-beam bombarded,[24] or ion implanted.[21,25,26] Recently, Solomon and Klein[27] reported an electroluminesce peak at approximately 5 eV observed in 1000-Å films of SiO_2, electrically stressed at either polarity to fields just below breakdown. No such electroluminesce was observed at lower stress fields. This peak could well be due to photons generated when electrons from the oxide conduction band are captured by the deep electron trap level which, in turn, has only been created at the highest applied field conditions. This evidence, together with independent observation of electron trapping in highly stressed thicker films of SiO_2,[16,23] strongly suggests that in thicker films, too, the breakdown mechanism is preceded by, and quite likely is initiated by, the newly generated deep electron traps localized near the electrode which is at the more negative potential. We can fairly say that in the thinnest of all films, where breakdown occurs below 8 v, no impact ionization can take place, and, therefore, the breakdown field of $\sim 3\times10^7$ V/cm observed in these films probably reflects a fundamental limit on bond strengths in the silicon-oxygen system. Ferry[28] suggested, on the basis of theoretical calculations, that hot-electron runaway should occur at fields typically around 3×10^7 V/cm. In thicker films, it is sufficient that the internal fields at any region of the oxide approach this magnitude for breakdown to be initiated. The potential distribution in the oxide just before breakdown would be approximately that shown by B in Fig. 15. On the microscopic level, one can expect any localized nonuniformities, impurities, defects, or mechanical stresses to weaken the bonding structure and cause the breakdown condition to occur at a localized field lower than 3×10^7 V/cm. Examining the data from many different batches of capacitors, it is found that at any given current level I, even capacitors from the same batch having a factor of 100 difference in value of $T_{BD}(I)$ have very close to the same value of $V_{in}(I)$ and of the ratio $\Delta V_{BD}(I)/T_{BD}(I)$.

Thus, the weaker capacitors in a batch experience the same initial stress field and the same rate of in-

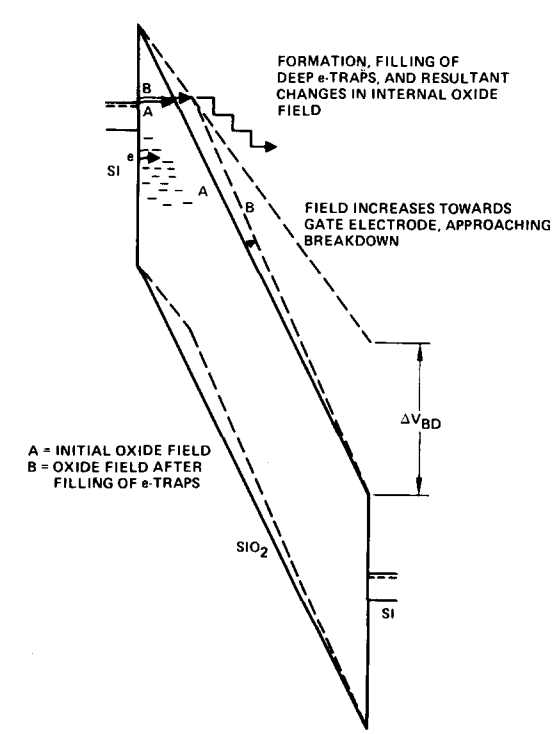

FIG. 15. Buildup of internal fields due to generation and filling of electron traps close to the injecting electrode.

crease of internal field [as measured by $\Delta V_{BD}(I)$ at the time of breakdown] as the longer-lasting capacitors, but the former break down at a lower level of internal field.

The exact nature of the generated e-traps is presently unknown, but they are most likely related to strained or broken Si-O bonds. The E_1' or C band observed in quartz and fused silica[26,29-31] is a deep (~5.8-eV) electron trap related to relaxed broken Si-O bonds or to oxygen vacancies. A second band, the B_2 center at ~5.0 eV, has been observed optically in ion-implanted SiO_2 [26] and has been related to displacement of network oxygen atoms. Also, still unclear is the mechanism by which the e-traps are generated. It appears that both a high stress field (which stressed the Si-O bonds and accelerates the electrons) *and* a high injection current are necessary. Although, in the present experiments, the high fields are always accompanied by a high injection current, the data of Fig. 8 and Table I suggests that the current density is the dominant factor. It is still necessary, though, for the high-field condition to exist for breakdown to occur, as can be seen from many internal photoemission measurements, where high injection currents at low fields do not normally result in breakdown.

The use of the constant current stress technique for yield studies can become a powerful tool in a MOS production environment because of its ease of implementation at the wafer level, its accuracy, and speed. However, as a tool for predicting long-term reliability effects, further studies must be performed which will show if and how the very-high-field stress results can be extrapolated to predict breakdown in MOS devices operating at very much lower oxide fields and current levels. The present work has shown that the time to breakdown (or dielectric strength) decreases strongly with magnitude of the oxide current, applied field, and temperature, and less strongly with oxide thickness. It may be that in going from fields $\gtrsim 1\times10^7$ to $\lesssim 2\times10^6$ V/cm, from oxide currents >10 to $<10^{-12}$ mA/cm^2, and from oxide thicknesses $\lesssim 200$ to >500 Å, a transition region would be traversed which would make it difficult if not impossible to relate data in the two ranges. The break in T_{BD} at t_{ox} 100 Å in Fig. 6 is a case in point.

The cumulative nature of the degradation under stress should be carefully considered when subjecting IC's to accelerated high-temperature high-voltage tests, which certainly weed out the weak parts, but also permanently weaken the oxide in the good parts (since no high-temperature anneal is possible for the packaged parts). This should also be of concern in the gate oxide of input gate protection devices, where occasional high-voltage spikes may not cause outright breakdown but will bring the device closer to breakdown under normal operating conditions. Devices exposed to electron or ion beams not followed by high-temperature anneals, such as in the e-beam-addressed mass memories (BEAMOS) or devices which rely on operation at a high field such as in high-voltage MOS switches, may also suffer a cumulative degradation effect.

VII. SUMMARY

A novel technique was described which was used to study the intrinsic breakdown mechanism in very thin films of thermal SiO_2. It was determined that high-field and high electron injection current conditions existing in the films just prior to breakdown result in the generation of a very high density of defects which electrically behave as stable electron traps. These traps are most likely generated close to the injecting electrode. The internal field due to electrons trapped in the oxide can approach 3×10^7 V/cm which appears to be the maximum field strength which Si-O bonding can withstand. Films stressed at 77°K exhibited an improvement by a factor of 10 in their time to breakdown relative to films stressed under identical conditions at 300°K. At all temperatures between 77 and 393°K, the breakdown mechanism is intimately related to the rate of generation of the electron traps. The experimental evidence suggests that trapped electrons rather than trapped holes increase the local internal field to the runaway limit. No evidence was obtained to support the impact-ionization breakdown model which, at least for films of thickness below 160 Å, must be seriously questioned.

The constant current technique was described also as a tool for studying yields of films of thermal oxide. It was found that under proper processing conditions the dielectric integrity begins to degrade only for film thicknesses below approximately 70 Å.

Still to be determined is the nature of the deep electron traps, which would also shed light on the mechanism of formation and possible methods of treatment to alleviate the problem in future generation VLSI MOS technologies. Further work is required in the intermediate range of stress fields (2×10^6 to 1×10^7 V/cm), oxide current (~10^{-6} A/cm^2), and oxide thickness (150–600 Å).

ACKNOWLEDGMENTS

The author gratefully acknowledges Dr. T. N. Toombs for his support and encouragement during this work. Helpful discussions were held with Dr. S. T. Wang, who also assisted with collecting the yield data. Particular acknowledgement is due W. Nielsen for invaluable assistance with the experimental setup and for patiently collecting the greater part of the voluminous data.

[1]Numerous articles have been published in the last few years to explain various theoretical and experimental aspects of breakdown in films of SiO_2. Two articles which have a good list of references in this subject are N. Klein, in *Advances in Electronics and Electron Physics*, edited by L. Maroon (Academic, New York, 1969), Vol. 25, p. 309 and B.K. Ridley, J. Appl. Phys. **46**, 998 (1975).
[2]N. Klein, J. Electrochem. Soc. **116**, 963 (1969).
[3]C.M. Osburn and D.W. Ormond, J. Electrochem. Soc. **119**, 591 (1972).
[4]C.M. Osburn and E.J. Weitzman, J. Electrochem. Soc. **119**, 603 (1972).
[5]D.Y. Yang, W.C. Johnson, and M.A. Lampert, 13*th Annual Proceedings on Reliability Physics* (IEEE, New York, 1975), p. 10.
[6]J.J. O'Dwyer, J. Appl. Phys. **40**, 3887 (1969).
[7]T.H. DiStefano and M. Shtazkes, Appl. Phys. Lett. **25**, 685 (1974).

[8]S. P. Li, E. T. Bates, and J. Maserjian, Solid State Electron. **19**, 235 (1976).
[9]P. Solomon, N. Klein, and M. Albert, Thin Solid Films **35**, 321 (1976).
[10]N. J. Chou and J. M. Eldridge, J. Electrochem. Soc. Solid State Sci. **117**, 1287 (1970).
[11]C. R. Barrett and R. C. Smith, Technical Digest of International Electron Devices Meeting, Washington, 1976, p. 319 (unpublished).
[12]E. Harari, Appl. Phys. Lett. **30**, 601 (1977).
[13]G. Lewicki, J. Appl. Phys. **47**, 1552 (1976).
[14]M. Lenzlinger and E. H. Snow, J. Appl. Phys. **40**, 278 (1969).
[15]R. Williams, Phys. Rev. **140**, A569 (1965).
[16]P. Solomon (private communications).
[17]E. Harari, S. T. Wang, and B. S. H. Royce, J. Appl. Phys. **46**, 1310 (1975).
[18]R. C. Hughes, E. P. EerNisse, and H. J. Stein, IEEE Trans. Nucl. Sci. **NS-22**, 2227 (1975).
[19]J. R. Srour, S. Othmer, O. L. Curtis, Jr., and K. Y. Chin, IEEE Trans. Nucl. Sci. **NS-23**, 1513 (1976).
[20]F. B. McLean, H. E. Boesch, Jr., and J. M. McGarrity, IEEE Trans. Nucl. Sci. **NS-23**, 1506 (1976).
[21]W. C. Johnson, Z. A. Weinberg, and H. S. Lee, Princeton University Technical Report RADC-TR-76-158, 1976, p. 17 (unpublished).
[22]M. H. Woods and R. Williams, J. Appl. Phys. **47**, 1082 (1976).
[23]C. S. Jenq and W. C. Johnson (private communication).
[24]C. T. Shih, Ph. D. dissertation (Princeton University, 1975) (unpublished).
[25]S. T. Wang, B. S. H. Royce, and T. J. Russell, IEEE Trans. Nucl. Sci. **NS-22**, 2168 (1975).
[26]G. W. Arnold, IEEE Trans. Nucl. Sci. **NS-20**, 220 (1973).
[27]P. Solomon and N. Klein, J. Appl. Phys. **47**, 1023 (1976).
[28]D. K. Ferry, Solid State Commun. **18**, 1051 (1976).
[29]E. W. J. Mitchell and E. G. S. Paige, Philos. Mag. **1**, 1085 (1956).
[30]R. A. Weeks and C. M. Nelson, J. Am. Ceram. Soc. **43**, 399 (1960).
[31]C. M. Nelson and J. H. Crawford, Jr., J. Phys. Chem. Solids **13**, 296 (1960).