

PATENT SPECIFICATION

DRAWINGS ATTACHED

Inventors: TOM KILBURN and FRANK HALL SUMNER

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COMPLETE SPECIFICATION

Improvements in or relating to Electronic Digital Computing Machines

5 We, NATIONAL RESEARCH DEVELOPMENT CORPORATION, 1, Tilney Street, London, W.1. a British corporation established by Statute. do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

10 This invention relates to electronic digital computing machines and is more particularly concerned with a machine as described in first co-pending Application No. 9300/60 (Serial No. 976,499) and in second co-pending Application No. 13854/60 (Serial No. 979632) wherein a main data word store of immediate or high access speed but of limited word capacity is employed in conjunction with a secondary data word store of much larger capacity but, usually, lower speed of access and in which means are provided for effecting automatic transfer of a block or group of a predetermined number of data word signals from the secondary store into the main store in the event that an order or instruction signal operative in the machine control system in performance of a normal computing programme calls for a programme data word address whose signal content is not, at that time, present in the main store.

30 As described in said first and second co-pending applications, the main store comprises a plurality of sections, such as magnetic core storage matrices, each capable of registering a predetermined number, or block, of data word signals and means in the form of a memory comparator circuit are provided for translating the programme address signal of the current order or instruction into a form suitable for effecting selection within the main store of the relevant block of storage locations containing the required single word storage

location or, alternatively, for providing an automatic transfer-initiating signal when the word block comprising the required word storage location is not present within the main store. 45

With such an arrangement it is usually necessary to clear one of the word block sections of the main store by transferring its existing data word contents to the secondary store in order to provide the necessary storage locations in the main store for receiving the respective data words of the new block which is to be transferred from the secondary store. This, in turn, involves the selection for such clearance of one of the plurality of block sections of the main store in a manner which is most suited to the future operation of the machine and which will avoid, as far as possible, transferring from the main store a block of data words containing any word which is likely to be required again in the near future since such renewed requirement would necessitate a further transfer of the just-transferred block back into the main store with the accompanying loss of useful machine operating time. 60 65

One possible and previously suggested mode of selection resides in the clearance, in readiness for each new secondary to main store transfer operation, of each main store block section in turn while another and also previously suggested mode is one in which selection of which main store block section is to be cleared is vested in the machine itself and is based upon the frequency of past-usage of each of the different main store block sections, the block section having the least frequent past-usage being that chosen for clearance. 70 75 80

An object of the present invention is the provision of a further alternative and advan-

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tageous mode of selection based upon an analytical examination of the usage history of each of the word blocks currently located in the main store and the selection, for clearance, of one block according to a choice determined principally by the respective periods of time during which each block has been located in the main store without use having been made thereof. To achieve the required analysis, a machine in accordance with the invention is so arranged that at each transfer operation, in addition to effecting the requisite clearance of a main store block storage location and the transfer of a secondary store word block thereinto, a special pre-transfer order programme is initially executed by which the above described choice is effected and by which, also, appropriate adjustment of certain registered transfer time and usage information is made in respect of each of the different main store word blocks.

In order that the nature of the invention may be more readily understood, one particular embodiment thereof will now be described by way of illustrative example only and with reference to the accompanying drawing, whose single figure is a block schematic diagram showing the principal components of an electronic digital computing machine including the invention.

The arrangements illustrated closely resemble those described in the aforesaid second co-pending application, except for the elimination of the particular form of block clearance selector device 50 described therein and the incorporation of further elements to be described later.

The machine about to be described is one arranged for operation in the parallel mode and with binary form numbers. Accordingly, where reference is made to a "multiple", such term is to be construed as meaning a group of separate conductors, one for each signalled digit value, while reference to "gate means" in association with such multiples is intended to mean the control by gate circuit means of all of the separate digit leads of the multiple by means of one or more control signals. Such multiples or conductor groups are shown in the drawings only as a single line while, in the interests of clarity, the various gate control signal connections and other elements have been omitted since their construction and arrangement follow the now well known forms and practices of the art.

The embodiment shown comprises a main or high access speed store 10, a secondary store 11, an instruction or order register 14 with an associated control register 44 for normal machine control purposes during execution of a computing programme, a separate transfer control register 17 and an associated transfer instruction register 47, a memory-comparator circuit 21 and an associated code signal generator 15, and a group of special

word and digit storage registers including a transfer instruction store 49, a main store block register 56, a secondary store directory register 63, a programme block directory register 70 and a so-called working store 52.

As it is a feature of this invention that an address as defined by the address digits of an instruction or order has no constant relationship to any one or any particular group of storage locations within the machine, it is pointed out that when, hereinafter, reference is made to a "programme" address number or a "programme" block number, the intention is to refer to the address digit configuration as used in the order or instruction of the programme for a particular computing operation being performed, whereas reference to a "store" block number or a "store" address, means the address identification of a particular word storage location or a particular group of separate storage locations within a particular piece of apparatus.

The main store 10 conveniently comprises eight magnetic core storage matrices each capable of registering 1024 data words in the form of 16 block of 512 words each. Address selection within the main store 10 is by address select means 12 which may comprise the usual diode tree circuits. Selection of a desired one of the 16 store block positions is affected by a group of eleven digit signals d_{12} — d_{22} of an address and applied by way of an input multiple 28. The similar selection of any desired single word storage location in any selected block in store 10 is effected by a group of nine digit signals d_3 — d_{11} of the same address and applied by way of input multiple 27. The write input multiple of the main store 10 is indicated at 41 and the read-out multiple at 42.

The secondary store 11 conveniently consists of one or more magnetic drum stores capable of providing 512 separate block storage locations available sequentially and each capable of registering a block of 512 separate words. Selection within the secondary store 11 is effected on a block basis only by address select means 16 which may again be of any well known form and include means for providing an output signal θ which is indicative of the store address of the next block storage location which will become available and is in the form of a group of address digit signals corresponding to those of register 14 for the same block. In addition, such address select means 16 include a coincidence testing circuit to which the said θ signal is applied for comparison with a block address signal fed to the input 20. When coincidence is established, a signal is emitted over lead 68. The said θ signal is also available externally on lead 60. The write input multiple to the secondary store 11 is indicated at 29 while the read output multiple is shown at 31. The latter is connected by way of transfer gate 22 to the

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write input 41 of main store 10 while the write input of the store 11 is fed through transfer gate 23 from the read output multiple 42 of the main store 10.

5 The precise form of the main and secondary stores is of no concern to the present invention.

10 The write input multiple 41 and the read output multiple 42 of the main store 10 are also connected in the usual way to highways 25 and 26 respectively feeding the other parts of the machine including the normal instruction and control registers 14, 44 and the computing circuits 59.

15 The instruction register 14 may be of any known form and provides the necessary address and function controlling signal outputs. This register 14 includes add or subtract means for combining a first instruction signal with a modifying signal in known manner. The normal instruction signal input is shown at 24 and the modifier signal input at 18. The usual decode circuits indicated at 45 provide the necessary control and other signals for operating the machine in accordance with the function digits of the applied instruction. The word and block address signal outputs are fed over multiples 33, 34 to the address select means 12.

25 The associated control register 44 is again of any suitable known form and can be set according to the digit configuration of an applied input signal on the multiple 80 and progressively altered during machine operation to define the address of the various successive orders of a programme. This control register is arranged to be capable of being immobilised by an input signal on lead 81 from switch device 46 referred to later. The respective word and block address defining digit signal outputs from this control register are also fed over multiples 33 and 34 to the address select means 12 in parallel with those from the instruction register 14.

30 The transfer control register 17 is similar to the register 44 and is also arranged to be capable of being immobilised by a signal from the switch means 46 over lead 82. This control register 17 is also arranged to be capable of being reset either to a first particular chosen digit configuration by reset device 48 or to a second chosen digit configuration by an alternative reset device 72. This transfer control register also includes the usual arrangements for progressively altering the control number stored therein after the end of each operation cycle so as, normally, to select the next order of the series. The various digit signal outputs from the control register 17 are applied over multiple 83 to the address select means of the transfer instruction store 49.

65 The transfer instruction register 47 is basically similar to that of the normal instruction register 14 and includes function de-

code means 84 operated by the function digit signals of an applied instruction to provide control potentials to various gate and other devices operative during the automatic transfer and time adjusting cycles. The instruction signal input to the instruction register 47 is indicated at 85 while the modifier input is shown at 86.

70 The memory comparator circuit 21 is described in detail in the aforesaid first co-pending application and effectively comprises sixteen separate banks of combined trigger and equivalence detecting circuits. One input to each equivalence detecting circuit is derived from the associated trigger circuit whereas the other input is provided by the related address digit signal of the block identifying group provided over multiple 34 from the instruction register 14 or the similar outputs of the control register 44.

75 Each trigger circuit in each bank of the memory comparator circuit is arranged to be set to one or the other of its two alternative states in accordance with the related digit value of the block identifying address signal, such setting inputs being fed by way of multiple 30 from the register 56. Each bank of the memory comparator circuit has an individual output lead 19 which is energised if, but only if, the setting states of all of the memory trigger circuits of that bank coincide with the applied digit signals on multiple 34. When such coincidence occurs, the corresponding output signal on the related lead 19 provides an input to the code signal generator 15 which is again of the form as described in the first co-pending application. This signal generator effectively provides, in response to energisation of any input lead 19, a 4-digit signal combination within the range 0000, 0001—1111 according to the particular bank of the memory comparator circuit 21 where coincidence has been established. Such 4-digit signal from the code signal generator forms the block identifying signal input to lead 28 of the address select means 12. In addition, the memory comparator circuit 21 provides an output on lead 37 when coincidence is established in any one of the banks or, alternatively, provides a non-equivalent output signal on lead 39 when there is failure to establish coincidence in any one of the banks of trigger circuits.

115 The register 56 is similar to that described in the aforesaid second co-pending application and comprises a multi-address word storage device of any convenient type, for example, a magnetic core store matrix, and its associated address select means 57 which again may comprise diode tree circuits of known form. This register has 16 separately identifiable storage locations, one for each of the block positions of the main store 10, and each is selectable through the address selection means 57 by the 4-digit main store block selecting 120 125 130

signal on multiple 28 by way of multiple 73. This register has a first read output at 87 and a first write input at 88. In addition, at each address position there is an additional and separate digit storage position for recording a 'use' digit related to the use or non-use of the corresponding main store block. 87a indicates the read output of this separate digit store while 88a indicates the write input. The read outputs 87 and 87a are connected over multiple 58 to the write input of the working store 52 while output 87 is also, as already mentioned, connected by way of multiple 30 to the setting input of the memory comparator circuit 21. The write inputs 88 and 88a are applied over multiple 89 from the read output of the working store 52. The input to the address selection means 57 also is capable of being supplied with controlling input signals over multiple 90 from the transfer instruction register 47.

The working store 52 is again a multi-address word storage device with associated address selection means 53. The write input to the store is indicated at 92 while the read out is indicated at 93. The address selection input at 94 is supplied over multiple 54 from the transfer instruction register 47. This working store is used as a temporary and operational storage during the various steps of the transfer and time adjusting operations and various exclusive address locations therein will be referred to later as work locations $w_1, w_2, w_3 \dots$.

The secondary store directory register 63 and the programme block directory register 70 are described in some detail in said second co-pending application, but as they do not perform any active part in the present invention they will not be further described.

As will be seen from the drawing, the respective address signal inputs to the address select means 62, 71 and 57 are all supplied through gate control means from the transfer instruction register 47. The read output 93 of the working store 52 is connected by way of multiple 67 to the address selection input 20 of the secondary store address selection means 16 and also to the write inputs of the registers 63, 60 and 56 and also by way of multiple 66 to the modifier input 86 of the transfer register 47 and by way of multiple 91 to the normal instruction register 14. Multiple 51 provides a connection from the block digit signal output of the instruction register 14 to the write input 92 of the working store 52 while the signal output 60 of the address selection means 16 is also connected to this write input 92, as are also the read outputs of the register 63, 70 and 56.

The transfer and time adjust instruction register 49 may be of any convenient form but as it is not normally necessary or even desirable to alter the form of any word stored therein, such store may be of fixed type com-

prising, for instance, a number of separate magnetic core devices having a removable magnetic core slug whereby the desired word configuration of each address location may be set by hand and not changeable otherwise. Such store has associated therewith address selection means 35 of any convenient form and whose address selection signal input is derived from the digit signal output of the transfer control register 17 over multiple 83.

The machine components so far described are those of the arrangements described in greater detail in the aforesaid second co-pending application to which reference should be made for further information.

The additional components provided to carry out the present invention comprise a counter device or "clock" 101, which is arranged to increase its count state or "time" value by one step each time the machine obeys an instruction by means of pulses supplied over lead 102 from the equivalence signal output 37 of the memory comparator circuit 21. The, continuously increasing, count state output of this clock counter 101 is connected by way of gate controlled multiple 103 to the write input 92 of the working store 52. A further, generally similar, counter device 104 is also supplied with input pulses from lead 102 and operates to count interval periods of, say, 1024 machine operations at which instant it provides an interrupt output signal Δt over lead 105 to operate the switch means 46 and to actuate the second reset device 72. At the next following pulse input it becomes reset automatically to zero to recommence counting. Its particular count state at any time is available, as the δt signal referred to later, by way of multiple 106 which also feeds the write input 92 of the working store 52. This interval counter is also capable of being reset to zero at any time by a pulse input over lead 115 from the non-equivalent signal lead 37 of the memory comparator circuit 21.

In addition to the modification of the main store block register 56 already referred to, three further multiple address registers 107, 108 and 109 are provided. Such registers are shown as separate entities on the drawing but in practice they may well be different portions of a single storage device such as a magnetic core storage matrix along with the other registers 56, 63 and 70.

Register 108 has 512 separate storage locations, one for each usable programme block address number; such addresses being selectable by address select means 110 under the control of the 11-digit block number signal on multiple 34 and supplied over multiple 111. The write input and read output of this register are connected respectively to the read output 93 and write input 92 of the working store 52.

Registers 107 and 109 each have sixteen

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separate storage locations, one for each block location of the main store 10; the address select means 112 of register 107 is supplied with the 4-digit code signal output of generator 15 over multiple 73 while the address select means 113 of register 109 is supplied with equivalent 4-digit signals by way of multiple 114 from the outputs of the transfer instruction register 109.

10 The normal machine computing circuits 59 are also made available for operational use during the periods when time value adjustments and choice of the main store block for clearance are being made by connection of the computing circuit inputs to the read output of the working store 52 and the corresponding connection of the computing circuit output to the write input of said working store.

15 Before describing the manner of operation of the arrangements described when concerned with the subject of the present invention, it is first pointed out that the manner of operation during both normal machine operation periods and during automatic transfer periods is described in some detail in the aforesaid second co-pending application and need not be dealt with here apart from stating that each normal machine operation involving use of one of the word blocks in the main store 10 results in the emission of the equivalent signal on lead 37, that the programme address of the used word block is at the same time signalled on the multiple 34, that the main store block in which such used word block is located is given by the code signal generator output on multiple 28 and that each transfer operation is preceded by the emission of a non equivalence signal on lead 39.

20 The register 49 now contains two separate groups or sub-routines of instructions, one commencing at address x dealing with adjustment of the timing records at each regular interrupt interval and the other, commencing at address y , dealing with both adjustment of the timing records and the automatic transfer and ancillary operations. Reset device 72, when operated, resets register 17 to number x , whereas reset device 48, when operated, resets the register to number y .

25 In each of the different 512 locations of the register 108 is registered a "clock time" value T_a which is the count state of clock counter 101 at that instant when the particular word block was last used in machine operation before it was transferred from the main store 10 to the secondary store 11. In each of the 16 storage locations of the register 107 is registered, at the instant when a 512-word block is transferred from the secondary store 11 into the related block location of the main store 10, a "time" value T_c , such value T_c being the count state of the clock counter 101 at the instant of transfer (T) less the value T_a (referred to

above) already registered in register 108 for the particular programme block being transferred. In each of the 16 storage locations of register 109 is registered a "time" value t which is determined in a manner which will be described below. In each of the single digit parts of the 16 storage locations of register 56 is registered a "use" digit, such digit being set to zero after each transfer operation or after each machine interrupt condition as described later and being set to value '1' immediately any word in that block location of the main store 10 is referred to during normal machine operation.

30 The manner of operation is as follows. During normal computing operation by the machine, each time an equivalence signal is emitted on lead 37 from the memory comparator circuit 21, the resultant pulse over lead 102 advances the clock counter 101 and the interval counter 104 by one step. Unless a call for an automatic transfer operation has occurred in the meantime, the interval counter 104 eventually reaches its maximum count condition at which time the output signal, Δt , on lead 105 therefrom causes a machine interruption by operating the switch 46 to transfer control from the normal control register 44 and instruction register 14 to the transfer control register 17 and the transfer instruction register 47 in a manner broadly similar to that described for automatic transfer operation in the aforesaid second co-pending operation. During such interrupt condition, however, the orders read from the transfer and time-adjust instruction register 49 comprise a difference series starting at a different number in the pre-set programme. This start number is automatically selected by operation of the reset means 72 by the same, Δt , signal on lead 105, instead of the reset means 48 of the transfer means, to cause the transfer control register 17 to be set at the proper number to select the first instruction of the sub-routine for dealing with such interrupt operation. Such series of interrupt orders comprises the selection under control of the transfer instruction register 47 of the successive address locations of the register 109 and the register 56. The "use" digit for address 1 in register 56 is first examined by transfer to the working store 52 and subsequent use of the computing circuits 59 to detect whether it is of value '1', indicating use in the immediately preceding period, or a value '0' indicating non-use in such period. If such examined digit value is '0', the existing time value t stored in the related address 1 of the register 109 is then altered by adding a number equivalent to the total count number, i.e. Δt , of the interval counter 104 thereto. This is effected by reading out such previous number t to a suitable address in the working store 52 and then transferring it to the computing circuits 59 together with a

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number signal representing the interval count number Δt to effect the addition of the two numbers and then transferring the answer number back to the same address 1 in the register 109, again by way of the working store 52. If, on the other hand, the said registered "use" digit value for the address 1 in the register 56 is of value '1', the previously existing time value t for such address 1 in the register 109 is erased whereby the value t becomes zero. The next instruction of the interrupt programme then resets the "use" digit for address 1 in register 56 to zero. The following instructions cause the same group of steps to be repeated for each of the separate addresses 2—16 in the registers 109 and 56.

Upon the occurrence of a demand for an automatic transfer operation, the manner of operation of which is described in the aforesaid second co-pending application, there is an initiating non-equivalence signal on lead 39 from the memory comparator circuit 21 caused by the non-coincidence of the applied programme word digits on multiple 34 with the setting states of any of the related banks of the memory comparator circuit. Such non-equivalence signal on lead 39 causes the operation of switch means 46 to transfer control from the registers 14 and 44 to the registers 17 and 47 exactly as described in the aforesaid second co-pending application and the simultaneous operation of the reset means 48 this time to alter the number set up in the transfer control register 47 to the address of the first of the alternative sub-routines of transfer control instructions held in the transfer and time-adjust instruction register 49. This second set of transfer instructions comprises those which are dealt with in detail in the aforesaid second co-pending application preceded by a group of further time adjusting and store block selecting instructions as follows.

The first time adjust time instructions of the group are substantially identical with those already described above for use under interrupt conditions whereby each of the 16 storage addresses in registers 109 and 56 is altered except that in this, transfer, case as the interval counter 104 has probably not reached its maximum value Δt , the particular count number at the moment δt which is a measure of the time intervals since the last interrupt or transfer operation is added to the existing number t in register 109 if the related use digit for the same numbered store block address in register 56 is zero.

The next instructions of the transfer sub-routine are concerned with the choice of the main store block which is to be cleared and these take the place of the previous instructions described in the aforesaid co-pending second application in which use was made of the selection signal output of the device 50 of that application.

The first instructions in the choice selection section of the programme sub-routine in the register 49 are concerned with an examination of the contents of each of the main store blocks 10 to see whether any one block is already empty. This is effected by the use of an instruction which reads the contents of the main word storage section of address 1 in the register 56 to a suitable address within the working store 52 from which, by the next instruction, such number is then fed to the computing circuits 59 where it is caused to be subtracted from zero. If the resultant answer is negative, it is indicative that the store is still occupied whereas a positive answer indicates that the said address is actually vacant. By the use of the well known conditional transfer technique, such presence of a positive answer is used to change the number of the transfer instruction register 47 by supply of a suitable number from store 52 over input lead 86 to a number which defines the address of the sub-routine in the register 49 of the first instruction of the actual transfer operation. If examination of address 1 fails to find it to be empty, the sub-routine so far described is repeated for each of the addresses 2—16 in register 56 in turn. Failure to find any one of the main store blocks already vacant is then followed by a further group of selection instructions in the register 49, the first of which selects address 1 in register 109 and transfers the content t thereof to a suitable space in the working space 52. This is followed by the selection of address 1 in register 107 and the transfer of the number Tc to another suitable address in the working store 52. By transfer of such numbers t and Tc from the working store 52 to the computing circuits 59 by further instructions in the register 49, the number Tc is subtracted from the number t to determine whether t is greater than Tc , evidenced by a positive answer. If the answer is positive, then by means of further orders using the known conditional transfer technique, the instruction register 47 is again advanced in number to the first instruction proper of the actual sub-routine. If, on the other hand, a negative answer is obtained for address 1, the same procedure is repeated for each of the further addresses 2—16 of the respective registers 109 and 107 until all have been examined and all have failed to show the presence of numbers t therein greater than the related values Tc . In the latter event, the time-adjust and transfer sub-routine in register 49 proceeds to a next group of test orders which determine in broadly similar manner whether the main store block 1 of the main store 10 has a recorded time value t (in register 109) which is not zero and in which the difference between the recorded value Tc in register 107 is greater than the value t in register 109. The answer to this operation is recorded on a

temporary address in the working store 52 and the same cycle repeated for each of the other addresses 1—16 of registers 107 and 109 with similar recording of the answers on fifteen further locations in the working store 52. In the event that more than one answer shows a positive value for $Tc-t$, then the two or more answers obtained are subtracted one from the other to determine which is the greatest and the store address showing such greatest value is then the one chosen for selection and clearance. To cover the possibility that no selected block has yet been found, the series of test and selection instructions in the transfer instruction register 49 includes a fourth group, the first order of which selects address 1 in register 109 and examines the value t therein for zero. Conditional upon such value being found zero, the recorded value Tc in register 107 is then transferred to a suitable address in the working store 52. A similar series of operations is performed for each of the other addresses 2—15 in the registers 107 and 109 and thereafter the various recorded values Tc which have been inserted in the working store 52 are examined by subtraction from one another to determine which is the greatest. The main store block corresponding to the address number in registers 107, 109 providing the largest value Tc is then the one selected for use in the subsequent transfer operation. Thereafter the sub-routine of instructions in the register 49 is concerned with the actual transfer operation itself and is as described in the aforesaid second co-pending application. As a prelude however to the actual transfer of the selected block from the main store 10 and its insertion in the secondary store 11, the address of such block, available on the multiple 34, is applied over multiple 111 to select the related address in the register 108 while the number Td on the related address position in the register 108 is first transferred to the working store 52 and then subsequently read from the working store into the selected address location of the register 108 to form a record of the clock counter setting at which the particular programme block about to be transferred was last used in the machine.

A selection by an analytical programme as described above has been found to take into account many of the often conflicting and variable factors concerned with the probability of future use of a block of data words which have previously been transferred into the main store, and to avoid, to a very large extent, the removal from such main store of any block of words which is likely to be required at an early time instant of the immediately following periods of machine operation.

The actual constructional arrangements employed may obviously be varied within very wide limits. For example, all of the various

registers 107, 108, 109 and 56 can form part of a single multiple address word storage device and may be part of the same device as the further registers 63 and 70. The machine is also capable of being arranged for serial instead of parallel mode operation.

WHAT WE CLAIM IS:—

1. An electronic digital computing machine which includes an immediate or high access speed main data word store, a secondary data word store of lower access speed, word transfer channels between said main and secondary stores and means for effecting transfer of required data words from said secondary store to selected storage positions in said main store and in which means are provided for effecting an analytical examination of the usage history of the data words currently held in each of the available storage positions in said main store in order to select said positions for receiving said required data words transferred from said secondary store.

2. An electronic digital computing machine according to claim 1 in which any data word currently held in said selected positions of said main store are transferred to said secondary store before said transfer of said required data words from said secondary store to said selected positions.

3. An electronic digital computing machine according to claim 1 or 2 in which said transfer operations are always concerned with block groups of a predetermined number of word storage positions in said main and secondary stores and in which said analytical examination of usage history is confined to each of said block groups collectively and not to individual word positions of any group.

4. An electronic digital computing machine according to claim 3 which includes a clock counter device whose count state is advanced by one step at each use of any word storage address of the main store during normal machine operation by a computing programme.

5. An electronic digital computing machine according to claim 4 which includes an interval counter device whose count state is advanced in unison with said clock counter device but which includes means by which its count state is reset to zero at each machine operation involving transfer of data words between said main and said secondary stores.

6. An electronic digital computing machine according to claim 5 in which said interval counter device is arranged automatically to reset to zero upon reaching a predetermined maximum count number and to provide an electric control signal indicative of such attainment of its maximum count number.

7. An electronic digital computing machine according to claim 6 which includes means operated by said control signal from said interval counter device to interrupt normal computing operation by the machine and to cause

alteration of statistical usage information related to said main store data storage positions.

5 8. An electronic digital computing machine according to any of the preceding claims 3—7 which includes a first multi-address signal storage device having a separate storage location for each of the block groups of data words held in said secondary store and in
10 which in each of said locations there is registered a count number Td which is the count state of said clock counter device at the instant when the block of data words related to said location was last used operatively in
15 the machine before it was transferred to said secondary store.

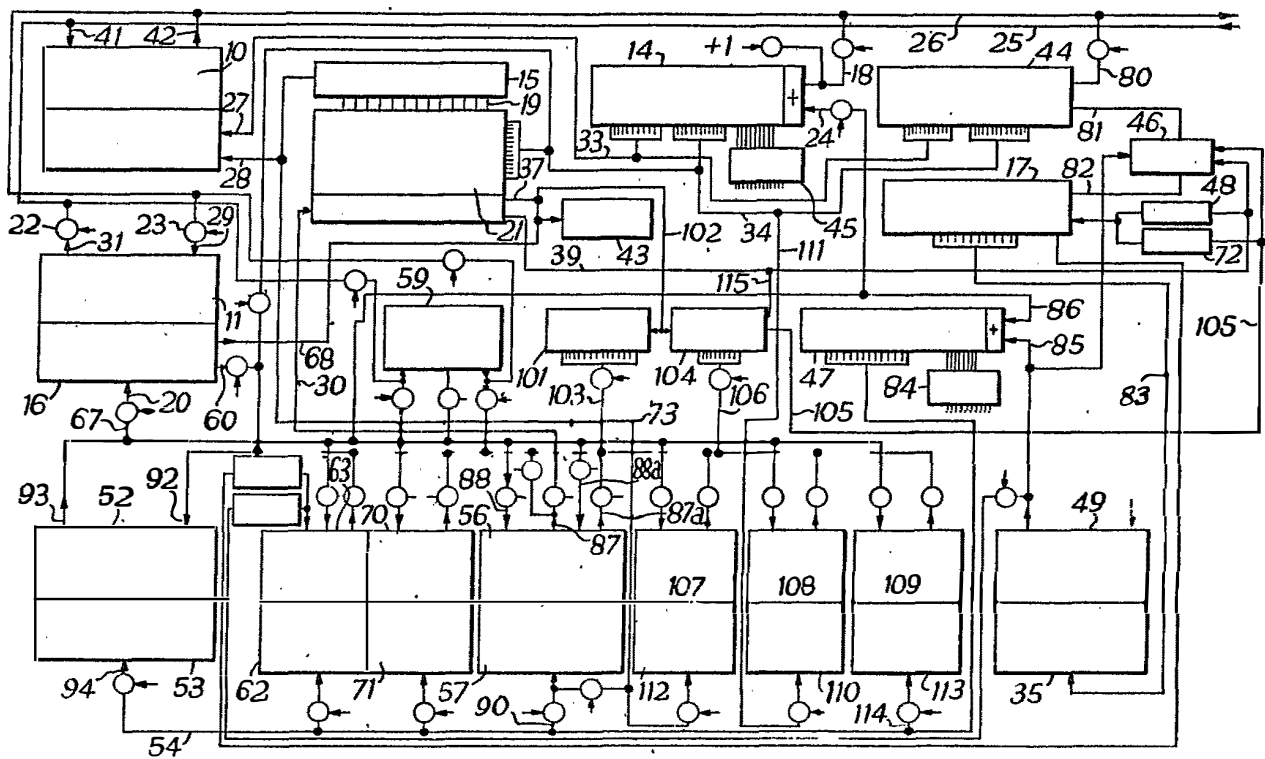
20 9. An electronic digital computing machine according to claim 8 which includes a second multi-address signal storage device having a separate storage location for each of the word block storage positions in said main store and in which in each of said storage locations thereof there is registered a number Tc which
25 is the count state of said clock counter device at the instant of transfer of the related data word block into the main store less the count number Td for the same data word block as registered in said first register.

10. An electronic digital computing machine according to claim 9 which includes a third register having a separate storage location for each of the word block storage positions in said main store and in which in each of said storage positions there is registered a signal indicating whether any word position of said word block
35 has been used operatively by the machine since a previous and predetermined time instant.

11. An electronic digital computing machine according to claim 10 which includes a fourth register having a separate storage location for each of the word block positions in said main store and in which in each of said storage positions there is registered a number t derived as hereinbefore described by examination of the storage position for the same word block
40 in said third register and said interval counter device.

12. An electronic digital computing machine substantially as described and as illustrated in the accompanying drawing. 50

POLLAK, MERCER & TENCH,
Chartered Patent Agents,
Audrey House, Ely Place,
London, E.C.1.
Agents for the Applicants.



979633 COMPLETE SPECIFICATION
 1 SHEET This drawing is a reproduction of
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