7.2 MOS-Addressed VFD Image Display on a Chip

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Introduction

A novel VFD (vacuum fluorescent display) image display, making use of low-energy cathodoluminescent phosphor elements together with an area cathode, has been investigated since 1976.[1)]

A first prototype TV display constructed of one driver per pixel was presented in 1980,[2)] and based on experimental results of a few memory pixels, the feasibility of incorporating memory functions in the panel was discussed.

This paper describes a miniature on-a-chip image display with 172(horizontal) x 108(vertical) integrated pixels in a 6 mm x 8 mm screen and also its peripheral circuits.

Experimental results, e.g., 10 fL screen brightness at 15 V driving voltage and power consumption of ca. 200 mW are described, and in addition the electrical driving techniques used to magnify part of the image for a magnitude of four times in area are also discussed.

The silicon chip includes horizontal and vertical shift registers in order to reduce the number of pins. This device is expected to be useful as a low powered view-finder-display for VTR cameras.

Design of the Display Device

The display device consists, in essence, of positive and negative sets of electrodes encased in a flat vacuum glass envelope. One set of electrodes, operated at positive potentials, consists of an array of picture elements aligned in an X-Y matrix. These picture elements are constructed from three MOSFET's and a capacitor. A light emitting phosphor element is deposited as a layer upon the drain of one of the three MOSFET's. The other set of electrodes constitutes an area cathode which consists of electron emitting fine filaments and an accelerating grid.

1. Memory pixel and screen

Figure 1 shows the circuit of the memory pixel. The pixel is composed of three transistors and a capacitor. The pixel has two modes, i.e., the display and the test mode. In the display mode, the transistor Tr3 is "OFF" and Tr1 is turned "ON". Then, the video signal is stored in the capacitor C through the data line D and Tr1. The video signal is held after the transistor Tr1 is switched "OFF". Electrons emitted from the filaments are accelerated by the grid potential, landing on the light emitting phosphor. The electron current is controlled by the gate voltage of Tr2, viz., the video signal.

In the test mode, Tr1 is "OFF" and Tr3 is "ON", thereby enabling the information on the storage capacitor to be read out onto the data line D. Using this scheme, any pixel can be easily tested.

The brightness B of a pixel is derived from the following equations.[3)]

$$B=K\cdot(Vp-Vdv)^{m}\cdot Ip^{n} \quad \cdots\cdots(1)$$

$$Vp=(Ip/b)^{1/k} \quad \cdots\cdots(2)$$

$$Ip=\beta(Vg-Vt)^{2}/2 \quad \cdots\cdots(3)$$

(when $Vg > Von$)

$$Ip=\frac{\beta}{2}(Von-Vt)^{2}\cdot 10^{(Vg-Von)/\delta} \quad \cdots\cdots(4)$$

(When $Vg \leq Von$)

Where

$$Von=Vt+2\cdot\delta/\ln 10 \quad \cdots\cdots(5)$$

and

$$\beta=\partial Ip/\partial Vg \quad \cdots\cdots(6)$$

K, m and n ; constants. Vp[2)]; the potential difference between the cathode and phospher electrodes. Vdv ; the dead voltage of the phospher. Ip ; the current at the phosphor electrode . b and K ; parameters in relation to the internal series resistance Ri between the cathode and phosphor electrodes. Vt, δ and Vg ; the threshold voltage, subthreshold coefficient and the gate voltage of the transistor Tr2, respectively.

Assuming the gate voltage of Tr2 to be equal to the video signal voltage, the calculated values of brightness versus video signal voltage are shown in Fig.2. The internal series resistance should be designed in consideration to the screen brightness, which depends on specific applications. In the case of view finders, the screen is viewed in the dark with no ambient light so that the brightness is not as significant as the uniformity and gray scale. The result of simulation indicates that high series resistance, shown by the solid line (C-3) in Fig.2, should be selected to assure a unifrom screen with good all-over gray scale chracteristics without using a mesh grid. The mesh grid would disturb the resolution when enlargement of the screen size is pursued by lenses.

The number of pixels is 172 x 108, and the screen size is about 6 mm x 8 mm. The pixel size is 46 μm x 54 μm, which can be enlarged to 4-9 times in area without significantly disturbing the characteristics as a view-finder-display.

2. Circuit design

In order to simplify the peripheral driving circuits and to reduce the number of pins, it is desirable that the silicon chip contains horizontal and vertical shift registers to scan the matrix array.

A single crystal silicon wafer, which has high mobility compared with other substrate materials, is utilized, since the horizontal shift register has to operate at a clock frequency in the order of 10^{6} Hz. Figure 3 shows a block diagram of the silicon chip. It contains 172 x 108 pixels and horizontal and vertical shift registers and analog switches to sample the video signal.

Set pulses ϕ_{HS} and ϕ_{VS} derived from the composite video signal are transfered by the horizontal and vertical shift registers, respectively. The output pulse from each stage of the vertical shift register selects the vertical position of the matrix array. The output pulse from each stage of the horizontal shift register opens the gate of the switching MOS to transfer the video signal to the pixel capacitor on the vertical select line. A dynamic circuit is used for the horizontal shift register in order to reduce the number of transistors. For the vertical shift register, a static circuit which is stable at low frequencies is used, since the vertical set pulse is transfered at a relatively low speed.

With the help of circuit simulation, device parameters such as channel length and width, capacitance etc. were determined upon the following constraints.

(1) The video signal should be stored in the capacitor within one clock period.

(2) The capacitor should be large enough to hold the video signal for one frame period.

Construction and Fabrication Processes

The construction of the image display is shown in Fig.4. A wiring pattern is formed upon a glass base plate. A thick film insulating layer is formed on the wiring pattern.

The silicon chip is fabricated by a p-channel silicon gate process using well-matured 5 μm design rules.

The formation of the phosphor screen is performed before separation of chips.

The phosphor screen formation process, which is based on electrophoretic deposition, was improved for industrialization.

The chip is die bonded with special silver adhesives.

Bonding of terminal pads on the silicon chip to the aluminium strips on the glass base plate is carried out by means of ultrasonic wire bonding.

The grid, which consists of a single rectangular metallic frame without a mesh, is mounted on the silicon chip circumference. A photograph of a portion of the phosphor screen is shown in Fig.5. The diameter of each phosphor element is made about 30μm to avoid charging problems.[4)]

Three fine cathode filaments, about 20 μm in diameter, are stretched over the chip, one of which being located over the center-line. The others are out of the screen area because they are located over the chip edges.

Sealing of the glass plate with the NESA coated face glass is performed in an atmosphere of inert gas with soldering frit. The NESA is held at the same electrostatic potential as the grid to assure uniform potential distribution and hence uniform internal series resistance.

Terminal pins are fixed to the glass plate with soldering metal. These are passivated by an extra molding agent to provide enough toughness for practical use.

A dual-in-line type package for mass production was fabricated, which is shown in Fig .6. Nevertheless it is possible to reduce the package size by using a single-in-line type of 28.0 mm (L) x 15.5 mm (W) x 5.0 mm (H) for some special applications.

Experimental Results and Discussions

1. Characteristics of the display device

A complete display device is shown in Fig.6. The dimensions of the filaments, grid frame, silicon chip and NESA coated front glass were analiezed carefully so that a uniform screen image could be realized by considering how the surface potential was affected by secondary electron emission and the electrostatic potential distribution over the screen.[4)] The brightness uniformity is within ±10 %.

Figures 7 and 8 show the characteristics of the screen brightness versus phosphor excitation voltage Vs and the grid frame voltage Vc, respectively. The brightness and the driving voltage ratings are chosen in accordance with the use of the device as a view finder. The grid voltage was set at the same as chip driving voltage.

The solid line in Fig.9 shows the characteristics of the screen brightness versus the gate voltage of Tr2 The calculation was made by using the theoretically estimated values of parameters. The calculated result was in good accord with the experimental curve, which is shown in Fig.9 by the dotted line.

The rating characteristics of the fabricated device are listed in Table 1.

2. Peripheral circuits

A block diagram of the peripheral circuits for driving the display device is shown in Fig.10. The peripheral circuits consist of three main parts, i.e., power supply, video amplifier and clock pulse generators.

The voltage converters transform the 9 volt power supply into a cathode voltage of 15 V and a filament voltage of 1.0 V.

The video amplifier inverts and amplifies the composite video signal.

In order to drive the display device, the clocks must be synchronized with the composite video signal. The clock pulse generator provides outputs of two sets of clock pulses, (ϕ_{H1}, ϕ_{H2}), and (ϕ_{V1}, ϕ_{V2}), which synchronize with the H-sync (horizontally synchronized) and V-sync (vertically synchronized) signals, and the set pulses ϕ_{HS} and ϕ_{VS} which are generated by delaying the H-sync and the V-sync, respectively. The system clock whose frequency is 7.2 MHz is generated by a crystal oscillator. The oscillation of the colck is triggered by the H-sync of the composite video signal.

As a small view finder for VTR cameras, it is desirable for the display device to have a resolution high enough to enable sharp focusing.

In the device, a quarter of the picture is easily magnified to full screen size by doubling the clock frequency.

In the magnified mode, a 7.2 MHz clock is used for the horizontal shift register of the display device. The clock for the vertical shift register of the display device is made by dividing the H-sync (The frequency : 7.8kHz). In the normal mode, the clock frequencies are divided by two. The input terminal M enables facilitates selection of either the normal or magnified mode.

3. Display of video image

Examples of displayed image of 6 mm x 8 mm are shown in Fig.11 (a) and (b). Figure 11 (b) shows the electrically magnified image of Fig. 11 (a). The experimental results for brightness versus video signal voltage are shown in Fig.12. The solid line and dotted line show the data for 3.6 MHz and 7.2 MHz horizontal shift register clock frequencies, respectively. These two curves and examples of displayed images show that an almost identical gray scale and contrast are obtained both in the display of normal and magnified image. A contrast of about 30:1 is derived from Fig.12.

Since the applied video signal is an analog, the gray scale cannot be defined exactly but 11 gray steps can be observed. The image was produced using the ITE standard gray scale chart and a home video cameras.

Though the emitted color of light from the ZnO:Zn phosphor has a broad peak at 505 nm, a black-and-white monochromatic image was obtained with a special plastic filter whose transparency was approximately 45 percent measured in footlambert. The image was enlarged up to about 1.5 inches by a lens with scarecely any disturbance in the display characteristics.

4. Testability

The design of the circuits enables every pixel on the wafer to be tested electrically enabling defective chips to be easily rejected before packaging. The feasibility of on-wafer electrical tests reduces the cost of the device because the testing cost is much less than that of the packaging. The results of visual tests after packaging of the display device match closely with those of the electrical wafer test.

5. Reliability

In the course of fabrication, items such as process parameters, passivation films, baking temperature and peripheral structure were studied to ensure reliability. The device parameters of silicon chips passivated with PSG or Si_3N_4 film were checked before and after the heating processes.A special molding agent on the terminal pins was developed to ensure the reliability. The wiring pattern was formed by aluminium thin film and a silver thick film periphery,

and both materials have good ohmic contacts by a covering of special graphite thick film. Several devices were fabricated by making use of such production processes, which were driven continuously for 1000 hrs in environments of 70°C and 90°C. The results shown in Fig.13 indicate that the reliabilty of the device is sufficient.

Environmental test procedures for automobile use (EIAJ-TF57-1) of conventional VFD's were conducted on many devices. The results proved that the device could be qualified to be put into practical use and the life would possibly be the same as that of conventional VFD's.

Conclusion

An on-a-chip VFD was developed as a view finder. It consists of such components as integrated memory pixels (172x108), a 6 mm x 8 mm screen and driving-circuits. The pixel size is 46 μm x 54 μm.

The silicon chip contains shift registers to reduce the number of pins and therefore it can be mounted in a 16 pin dual-in-line package.

The design makes it possible to test any pixel on the wafer, thus reducing costs.

The relation between the brightness and the video signal was estimated and the device parameters were determined with the help of circuit simulation before the fabrication of the display device.

The shape and structure of the cathode and the grid were carefully examined so that a uniform screen with good gray scale characteristics was obtained without using a mesh grid. The screen contrast is about 30:1.

The display device operates on 15 V, consuming ca. 200 mW and yields ca. 10 fL screen brightness.

A quarter of the picture is easily magnified to full screen size by the peripheral circuits. The power consumption of the display device including the peripheral circuits is ca. 800 mW. In the future, power consumption can be reduced by integrating the peripheral circuits on a separate silicon chip.

Finally, reliability test proved that the device is qualified for practical use.

Acknowledgement

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References

1. S.Uemura, U.S.Patent 4081716.
2. S.Uemura,et al., IEEE Trans. Electron Devices, vol.ED-28,No.6,pp.749-755,1981.
3. P.Goldberg, Luminescence of Inorganic Solids. New York:Academic, 1966,pp.685-710
4. S.Uemura, in Electrochem. Soc. Washignton D.C. Meeting,to be published, 1983.

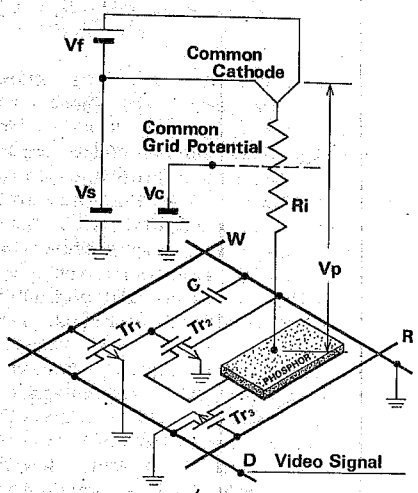


Fig.1. Circuit of the picture element.

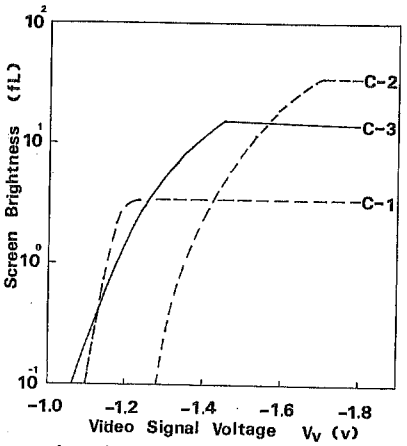


Fig.2. Screen brightness versus video signal relation for several series resistances.

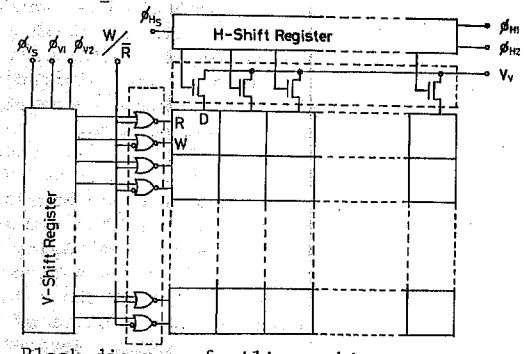


Fig.3. Block diagram of silicon chip.

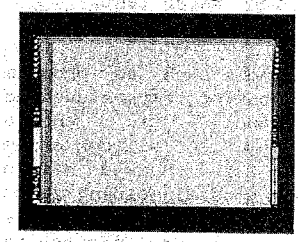


Fig.5.(a) Silicon chip with phosphor screen.

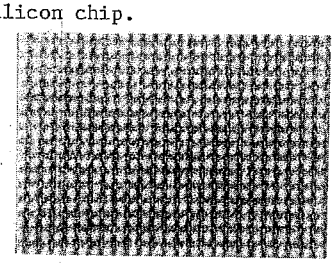


Fig.5.(b) A portion of the phosphor screen.

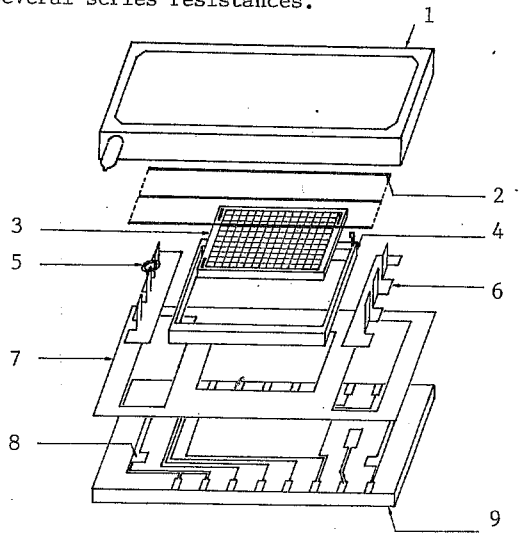


Fig.4. Construction of the on-a-chip image display: 1)face glass with NESA;2)filament cathodes;3)silicon chip;4)metalic frame;5)getter;6)supporting electrode for cathodes;7)insulating layer;8)wiring pattern;9)glass base plate.

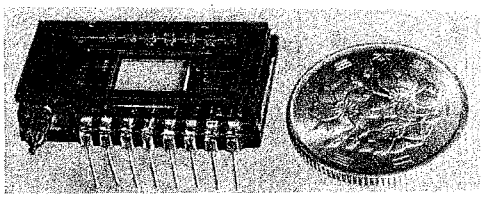


Fig.6. Photograph of the display device.

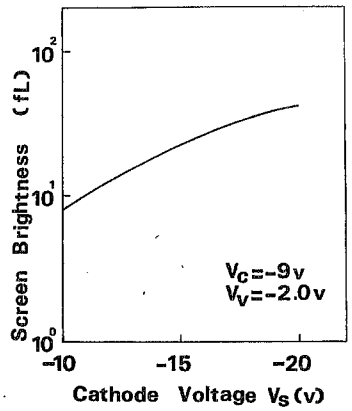


Fig.7. Screen brightness versus cathode voltage relation.

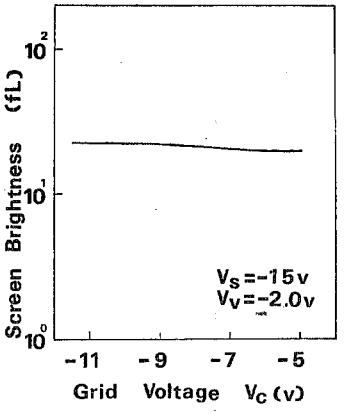


Fig.8. Screen brightness versus grid voltage relation.

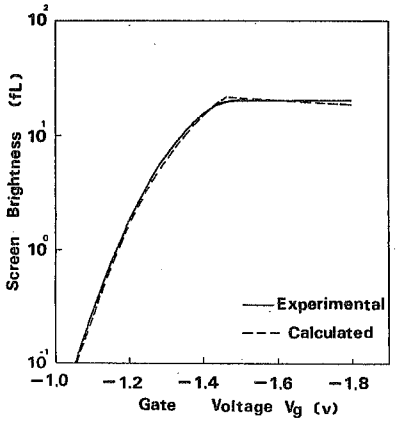


Fig.9. Comparison between experimental and theoretical results of screen brightness versus video signal relation.

Table 1. Physical Specification, Electrical Ratings and Characteristics of the device.

Chip Size	8.95(H)X6.31(V)mm^2
Display Area	7.912(H)X5.832(V)mm^2
Number of Pixels	172(H)X108(V)
Pixel Pitch	46 μm along H axis 54 μm along V axis
Phosphor Element Size	ca. 30 μm ϕ
Package Size	29.0(L)X18.0(W)X7.0(H)mm^3 16pin, Dual-in-line with a Exhaust Pipe.
Driving Voltage	-9V (Chip, Grid) -15V (Cathode) 1.0V (Filament)
Power Consumption	ca. 200mW ca. 800mW (with peripheral ccts.)
Screen Brightness	ca. 10 fL
Gray Scale	Analogue (>11)
Contrast	30 : 1

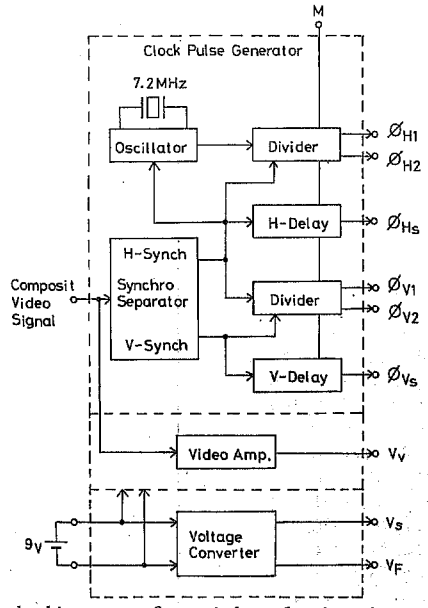
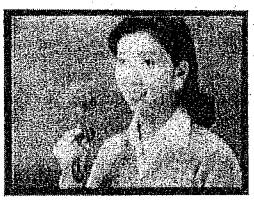


Fig.10. Block diagram of peripheral circuits.



(a) Normal

(b) Magnified

Fig.11. Photographs of displayed images.

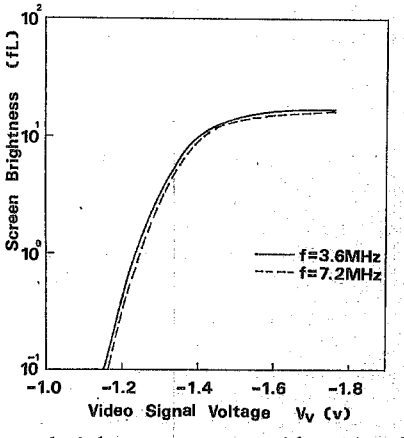


Fig.12. Screen brightness versus video signal relation at frequencies of 3.6 and 7.2 MHz.

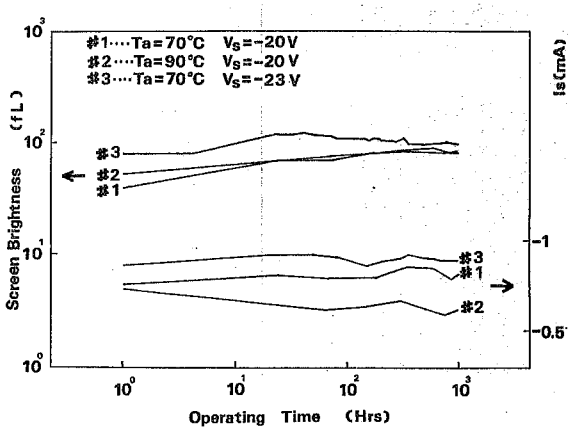


Fig.13. Results of reliability tests.