Esaki Diode High-Speed Logical Circuits*

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Summary—Logical circuits using Esaki diodes, and which are based on a principle similar to parametron (subharmonic oscillator element) circuits, are described. Two diodes are used in series to form a basic element called a twin, and a binary digit is represented by the polarity of the potential induced at the middle point of the twin, which is controlled by the majority of input signals applied to the middle point. Unilateral transmission of information in circuits consisting of cascaded twins is achieved by dividing the twins into three groups and by energizing each group one after another in a cyclic manner.

Experimental results with the clock frequency as high as 30 mc are reported. Also, a delay-line dynamic memory and a nondestructive memory in matrix form are discussed.

Introduction

ESAKI DIODES, which are also known as tunnel diodes, are highly suitable elements for logical circuits in view of their extremely high frequency limit, compactness, high stability, and low power consumption. Moreover, the cost can be expected to be very low for mass production quantities in the near future.

An Esaki diode is a two-terminal negative resistance element which is essentially bilateral. Therefore, unlike ordinary transistor switching circuits, Esaki diode circuits require that some special method be incorporated to obtain a unilateral characteristic for the transmission and amplification of digital signals. This situation is completely analogous to that which has been encountered in the case of the parametron.

To illustrate the application of Esaki diodes to logical circuits, a system closely related to the logical principles of parametrons will be discussed in this paper. This system of circuitry for Esaki diodes, based on a proposal by E. Goto, has been developed at the University of Tokyo with the cooperation of the Takahasi Laboratory of the Physics Department, the Amemiya Laboratory of the Applied Physics Department, and the Moto-oka Laboratory of the Electrical Engineering Department. An experimental model whose clock frequency is as high as 30 mc has been successfully built.

The Basic Principle

A typical voltage-current characteristic of an Esaki diode is illustrated in Fig. 1. It clearly shows the negative resistance region between A and B which is the

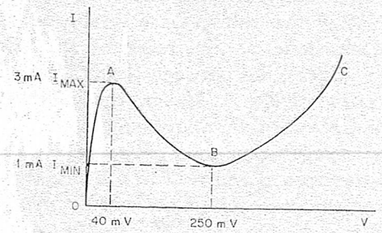

Fig. 1—A typical characteristic of a silicon Esaki diode.

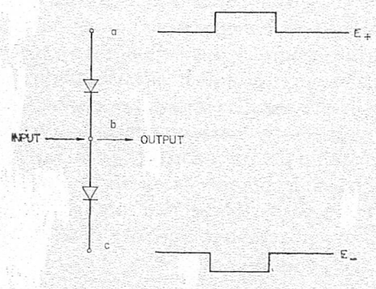

Fig. 2—Basic circuit named "twin."

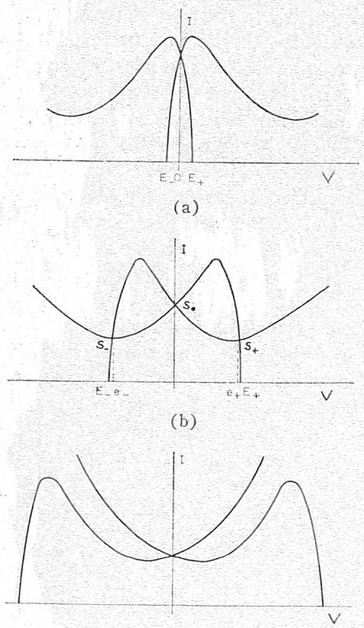

Fig. 3—Response curves of a twin.

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characteristic feature of Esaki diodes. Two Esaki diodes which have almost the same characteristic are connected in series to form the basic circuit shown in Fig. 2, which will be called a "twin circuit" or more simply a "twin." Symmetric exciting voltages E_+ and E_- of equal magnitude and of opposite polarity are applied between a and c. Depending on the magnitude of these exciting voltages, the twin shows three different kinds of response. When the voltages are small, the operating point of each diode, as illustrated by the two curves shown in Fig. 3(a), lies between O and A on the characteristic curve of Fig. 1. Hence, the potential at the middle point b is zero. Similarly, when the voltages are very large, the operating point of each diode of the twin circuit lies between B and C of the characteristic curve (Fig. 1) and the potential of the middle point b is also zero as shown in Fig. 3(c). When the voltages are chosen so that the operating points of both of the diodes of the twin lie between A and B as shown in Fig. 3(b), there are three possible operating points, S_0, S_+, and S_-. The operating point S_0 corresponds to zero potential at the middle point b, and it is unstable because both diodes are in the negative resistance region. Hence, the operating point of the twin diodes will go to either one of the two stable points, namely, S_+ or S_-, which indicates two possible potentials e_+ and e_- at the middle point b of the twin. These two potentials e_+ and e_- have equal magnitude but opposite polarity. A binary digit can be represented by these two potentials in a twin circuit.

When the exciting voltages are switched from a small value corresponding to the case shown in Fig. 3(a) to a value corresponding to the case in Fig. 3(b), the state S_0 having zero potential at the middle point of the twin will become unstable. The potential must flip to either of the two stable values e_+ or e_- [Fig. 3(b)], and these two should be equally probable for a twin consisting of well matched diodes. Under these circumstances, a very small signal applied at the middle point b will be sufficient to control the choice between the two possible states mentioned above. When the square waves shown in Fig. 4(a) are impressed on the twin as exciting voltages E_+ and E_- together with a small control signal $\pm E_n$, the two permissible voltages e_+ and e_- will build up as shown in Fig. 4(b). This process may be regarded as the amplification of the small input signals $\pm E_n$.

Intercoupling the middle points of the twins with each other by means of coupling resistors, logical operations and the transmission of information will be performed in just the same manner as has been done in parametron (subharmonic oscillator) circuits. Unilateral transmission of information will be accomplished by dividing the twins into three groups, I, II, and III, and exciting each group with one of the exciting signals, $E_{I\pm}$, $E_{II\pm}$, and $E_{III\pm}$, which are switched on and off one after another in a cyclic manner as shown in Fig. 5. The direction of information flow will be from group I to II, II to III, and III to I.

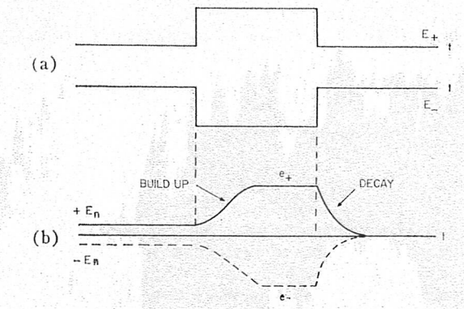

Fig. 4—Switching waveform of a twin.

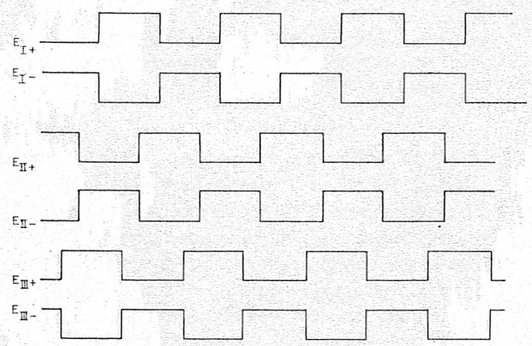

Fig. 5—The three phase exciting voltages.

Majority operations can be performed by a circuit shown in Fig. 6(a). The output of three twins X, Y, and Z in group I is applied to a twin U as its input signal. As the algebraic sum of the three signals from twins X, Y, and Z gives us the effective input of U, the state of U, which represents a binary digit u, is determined by the majority of the three binary digits x, y, and z, represented respectively by the polarity of the potentials of the middle points of twins X, Y, and Z.

Hereafter, in order to simplify the schematic circuit diagrams, we shall use the same conventions as those used for parametron circuits; that is, each twin will be represented by a small circle. Each pair of circles will be connected by a line when corresponding twins are coupled, one line being used per unit coupling intensity. In each circle representing a twin, the input coupling lines will come into the left side of the circle and the output will go out from the right side of the circle. Instead of showing the existing voltages explicitly, Roman numerals I, II and III will be written above the circles to indicate the kind of exciting voltages (cf. Fig. 5) being used.

AND and OR operations can be regarded as special cases of the majority operation with a constant bias. A symbol + will be inscribed in the circle representing a twin to indicate a constant input of unit intensity cor-

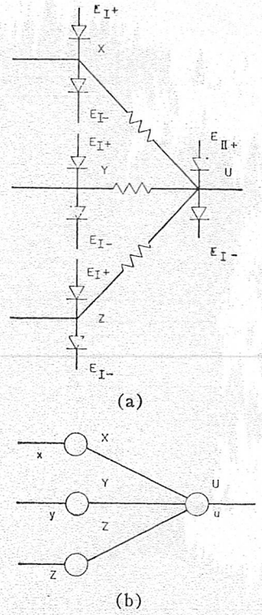

Fig. 6—The majority logic.

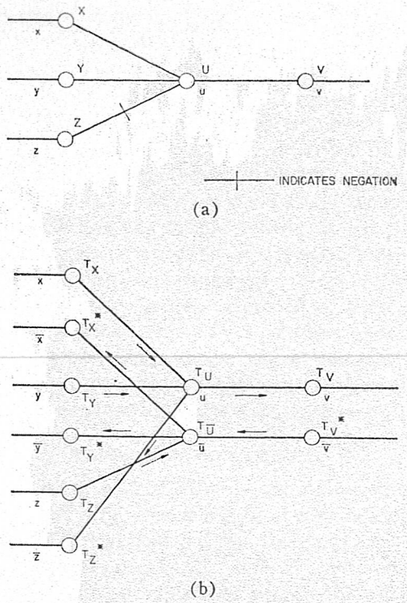

Fig. 7—(a) A majority operation with negation. (b) Negation in symmetric circuitry.

responding to a binary digit "1," and a symbol − will be inscribed to indicate a constant input of unit intensity corresponding to a binary digit "0." Accordingly, a circle with + having two input lines represents an OR circuit and a circle with −, an AND circuit. Using these conventions the schematic diagram of the circuit of Fig. 6(a) is shown in Fig. 6(b).

Negation or the NOT operation is another basic operation indespensable for general purpose logical circuits. In the Esaki diode twin circuits, however, we shall encounter some difficulties in making a NOT circuit. A NOT circuit changes a binary digit "1" into "0" and "0" into "1," and this means the reversal of polarity of dc signals in the Esaki diode twin circuits. In parametron circuits, since the signals are pure alternating currents, the reversal of the polarity is made simply by means of phase reversing transformers. In twin circuitry, since the signals are direct currents, obviously, transformers cannot be used for the reversal of their polarity. Of course, vacuum tube or transistor amplifiers can be used for reversing the polarity. These amplifiers, however, will cause serious signal delay, which makes these amplifiers unfavorable for extremely high speed operation.

In the twin or Esaki diode circuitry, it is possible to make the NOT operation without a delay by employing a rather elaborate system which may be termed the symmetric or push-pull system. In this system, a pair of two twins are used in a push-pull manner so that when one twin in a pair is holding a certain binary variable x, the other twin in the pair holds the complement $\bar{x}$. For example, the logical circuit shown in Fig. 7(a) is a circuit for making the majority u of three variables x, y, and (not z), and for transmitting u to the next stage v. This logical operation will be carried out by the circuit shown in Fig. 7(b), in which the pairs of twins representing binary variables x, y, z, u, and v are denoted by T_x, T_x*; T_Y, T_Y*; T_Z, T_Z*; T_U, T_U* and T_V, T_V*. It can be seen from the figure that by setting up the symmetric configuration once at the input, the entire circuitry of a machine can be constructed in the push-pull configuration. Calling the twin in a pair with no asterisk the front (push) twin, and the other (with asterisk) the back (pull) twin, a coupling line without negation in the logical diagram [Fig. 7(a)] may be interpreted to require coupling between corresponding front twins and between corresponding back twins. A coupling line with negation may be interpreted as the cross coupling between the corresponding front twins and the opposite back twins.

The increase of number of elements is obviously a disadvantage of this symmetric system. On the other hand, besides the speeding up of negation, there are two other interesting advantages of the symmetric system. One is its single significant error detecting property. An erroneous operation in either T_Z or T_Z* in Fig. 7(b) will be called significant if $x=\bar{y}$ and $\bar{x}=y$ hold. The presence of an error in this case will be detected by the fact that $v=\bar{v}$ at the twins T_V and T_V* in the last stage. On the other hand, if $x=y$ and $\bar{x}=\bar{y}$, the final result will be $v=x=y$ and $\bar{v}=\bar{x}=\bar{y}$ independently of z and $\bar{z}$. Hence, an erroneous operation of twins T_Z and T_Z* will not have any significance in the result of the computation. Suppose we have a large scale computer made entirely of

this symmetric scheme. Then, an erroneous operation of a twin in the accumulator will be significant if it occurred just before printing out of the accumulator content, and it will not be significant if it occurred just before the content is reset to zero. Therefore, it will be possible to detect significant errors by providing a relatively small number of comparators at the output stage of a large scale computer.

The other advantage is that the signal currents will be balanced perfectly in the symmetric system as shown in Fig. 7(b). In very high speed computers, spurious signals induced by common ground currents would be a very serious problem. By placing the twins in each pair closely together in the symmetric system, the ground currents will be balanced out, and the undesirable effects of ground currents can be completely eliminated.

Experimental Results

An experimental model of a binary counter using the symmetric system has been successfully built. The logical diagram of the circuit is shown in Fig. 8(a), and the complete circuit in Fig. 8(b). In Fig. 8(a), 1, 2, and 3 form a flip-flop circuit to absorb the undesirable effects of chattering in the input switch. 4, 5, and 6 form a so-called digital differential circuit and a single pulse is obtained at 6 each time the state of the flip-flop changes from "0" to "1." 7, 8, 9, and 10 form a binary counter. Therefore, each time the input switch is switched from − to + the binary counter changes its state.

In Fig. 8(b), the input is connected to an asymmetric circuit and it is connected into a symmetric form between 1 and 2* and between 4 and 5* by NOT circuits. For the NOT circuit, both transistor amplifiers and transformer circuit shown in Fig. 9 were tested and both operated successfully. In Fig. 9, as the input to the twin in group II is only one, the transformer without dc restration can be used for negation. However, in this case the negation is accompanied by one stage of delay.

The equivalent circuit of an Esaki diode is shown in Fig. 10. The resistance with an arrow represents the dc characteristic shown in Fig. 1; C is the parallel capacitance, and R_s is the series resistance. The maximum switching speed will be determined by the time constant $\tau=C|-r|$, where $|-r|$ is the minimum of the absolute magnitude of the negative resistance.

Using silicon Esaki diodes made by the Sony Corporation, Tokyo, of which the specifications are $I_{max}=3$ ma, $|-r|=100$ ohm, $C=400$ pf, $\tau=4.10^{-8}$ second, and using coupling resistors of 2000 ohm, the binary counter circuit of Fig. 8(b) has been operated at 1 mc. Similarly, using germanium Esaki diodes (made by the Sony Corporation) of which the specifications are $I_{max}=3$ ma, $|-r|=10$ ohm, $C=40$ pf, $\tau=4.10^{-10}$ second, and using coupling resistors of 500 ohms, the same counter circuit has been operated successfully at the clock frequency of 30 mc. The frequency was limited to 30 mc because of the characteristic of the oscilloscopes presently available at the University of Tokyo. By comparing the time constants τ of both diodes, it seems possible to obtain a clock frequency as high as 100 mc with the present germanium Esaki diodes.

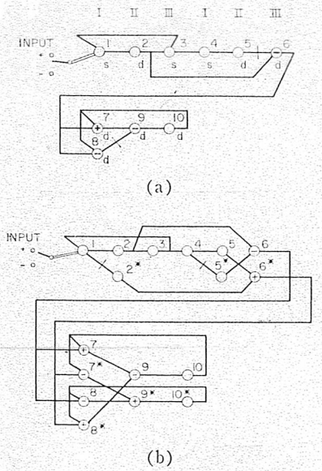

Fig. 8—(a) A binary counter with logical input. s indicates asymmetric circuits. d indicates symmetric circuits. (b) Full circuit diagram of Fig. 8(a).

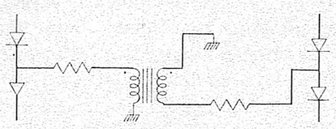

Fig. 9—NOT circuit by transformer.

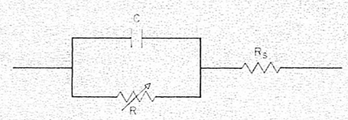

Fig. 10—Equivalent circuit of Esaki diode.

In these experiments the value of the coupling resistances have been determined so as to ensure a logical gain (the maximum number of inputs+outputs) of 10. From these experiments one may observe the fact that the relation between clock frequency f of the twin circuitry and the time constant should be given approximately by $f\cdot\tau\simeq 8$ to 25. This fact implies that the future development of better Esaki diodes having time constants of less than $4\cdot 10^{-11}$ second would result in a billion bit rate (1000-mc clock) machine.

Exciting power supply circuits used in the experiments are shown in Fig. 11. Instead of the square waves shown in Fig. 5, a superposition of dc biasing voltages

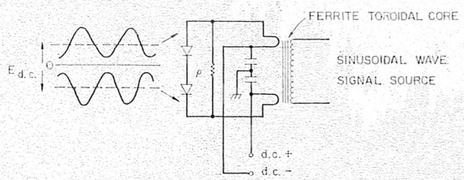

Fig. 11—Exciting voltage supply circuit

and pure sinusoidal voltages is used. The resistor ρ(20 ohms) is used for reducing the source impedance, and most of the source power (about 1 mw per twin circuit) is consumed by this resistor.

One of the important facts in the Esaki diode twin circuitry is the balance between the diodes. The maximum gain and stability depends critically on the balance. It is found that balancing I_{max} of the diodes is most critical. In our experiment, I_{max} in a twin was matched within ± 3 per cent tolerance to insure the operation of the counter [Fig. 8(b)] consisting of seventeen twins. The dependence of the balance on the parameters of diodes has been investigated by using the parametron digital computer (PC-1) which simulates the Esaki diode circuitry. The results will be published in the near future.

Memory Circuits

Two kinds of memory devices using Esaki diodes have been tested. The one is a serial delay-line memory proposed by E. Goto. The circuitry of this memory is shown in Fig. 12. A coaxial delay line cable with an open reflecting end is connected to the middle point of a twin. The state of the twin is controlled by the reflected signals, and a circulating dynamic memory circuit is formed. A 16-bit memory circuit at a 30-mc clock frequency using standard coaxial cables (75-ohm impedance, 5-mm diameter, and polyethylene filled) has been operated successfully. This delay line memory will be suitable for serial type computers.

The other is a nondestructive readout matrix array of diode twins proposed by K. Murata. Fig. 13 shows the basic circuit for each binary digit which is inserted at the cross point of an X-Y matrix array. In the normal state, dc holding signals (of value corresponding to Fig. 3(b)) are applied to A_+ and A_-. The nondestructive readout is made by varying the voltage of one of the X lines A_+ and A_- and by sensing the polarity of variation of the current in the Y line or lines. A double coincidence writing is effected by varying the voltage of A_+ and A_- of an X line to facilitate the change of the state

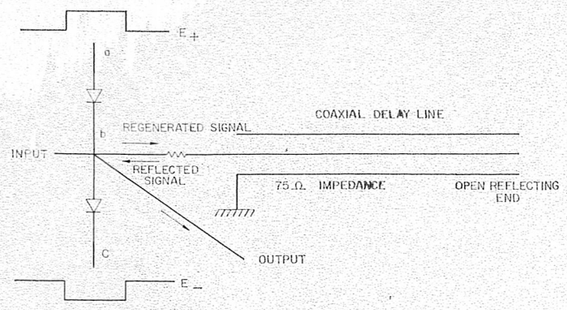

Fig. 12—Delay-line regenerating memory.

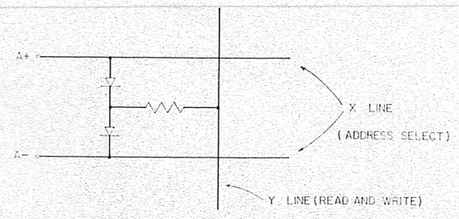

Fig. 13—A twin diode memory cell.

and by applying a writing voltage to a Y line. The results of tests made on a single basic unit are very promising. However, the number of Esaki diodes available at the present has been insufficient to build a full scale experimental matrix.

Acknowledgment

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