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(54) **LOW NOISE AMPLIFIER**

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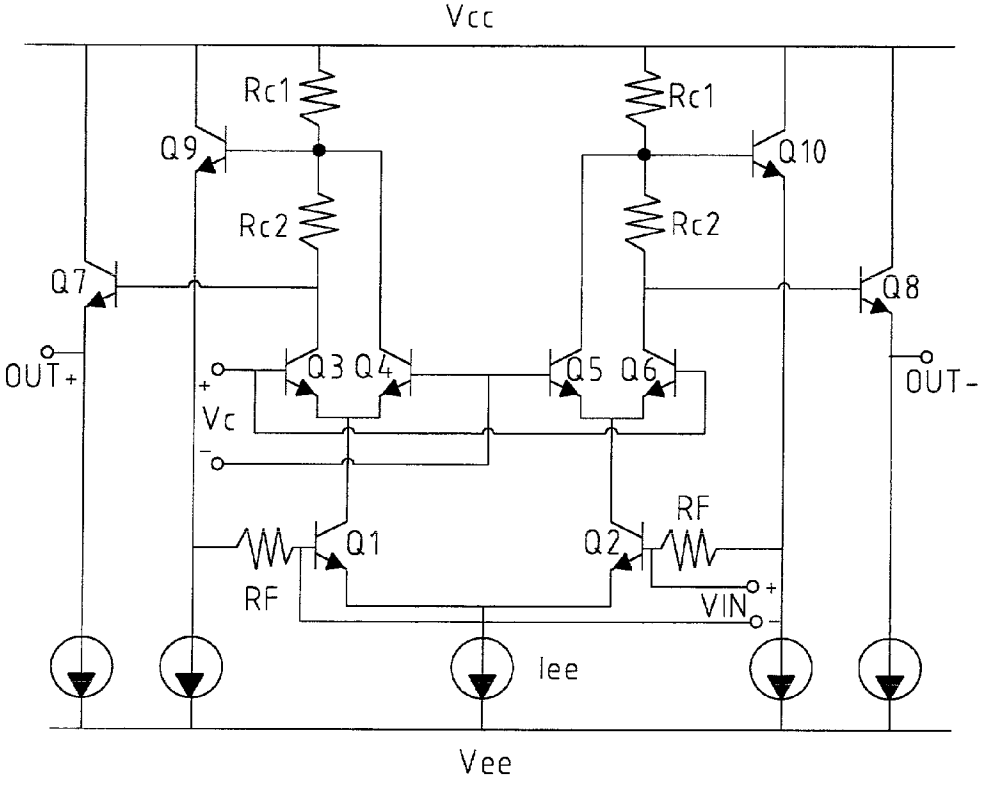
(57) **ABSTRACT**

It is shown a low noise amplifier comprising a first circuit block suitable for converting a first amplifier input voltage signal into current, a second circuit block adapted to divide the current coming from said first block, said second block being controlled by a second voltage signal, said first and second blocks conferring a variable voltage gain to the amplifier. The amplifier comprises at least one first and at least one second resistors and a feedback network, said at least one first resistor connected with one first output terminal of said second block and with a supply voltage, and said at least one second resistor being connected between said at least one first and at least one second output terminals of said second block, and said feedback network being coupled with said at least one first terminal and with said first circuit block, and said at least one second terminal being coupled with at least one output terminal of said low noise amplifier. (FIG. **3**).



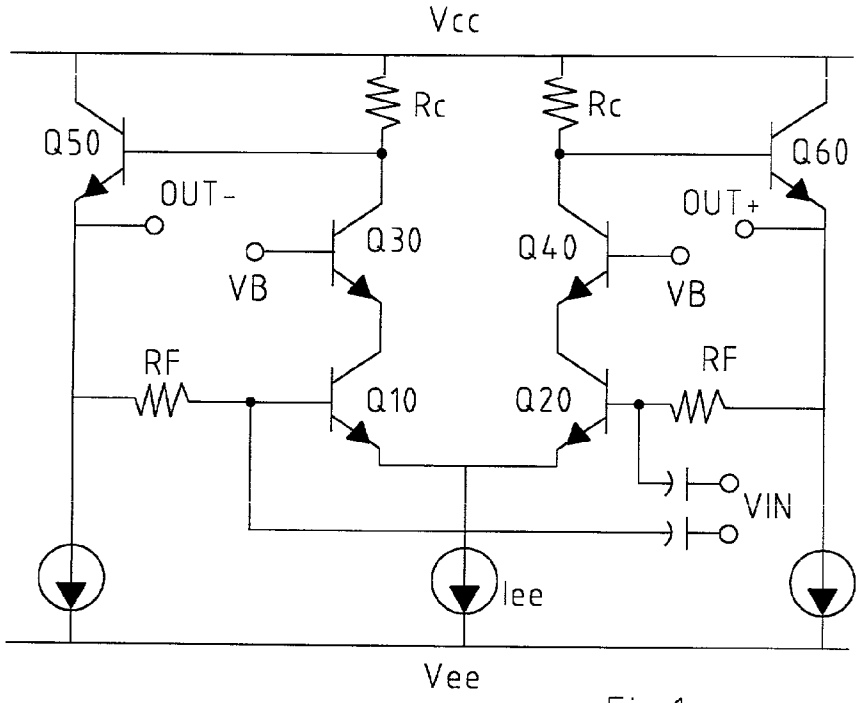

Vcc
Rc
Rc
Q50
Q60
OUT-
OUT+
Q30
Q40
VB
VB
RF
RF
Q10
Q20
VIN
Iee
Vee

Fig.1

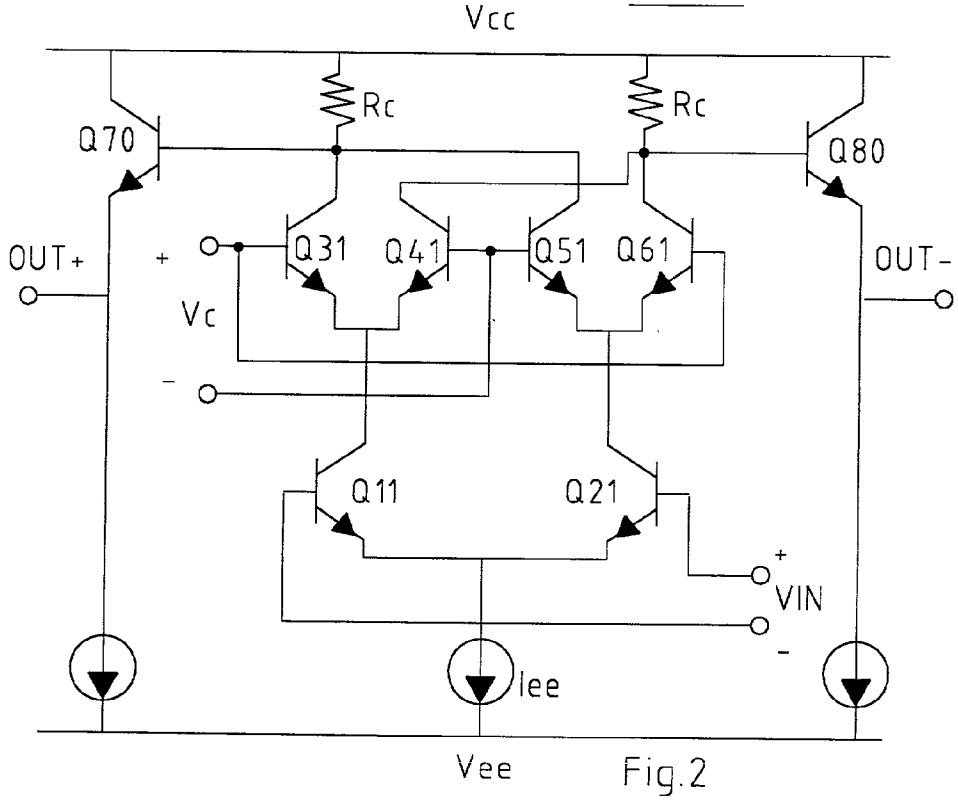

Vcc
Rc
Rc
Q70
Q80
OUT+
OUT-
+
Q31
Q41
Q51
Q61
Vc
-
Q11
Q21
+
VIN
-
Iee
Vee

Fig.2

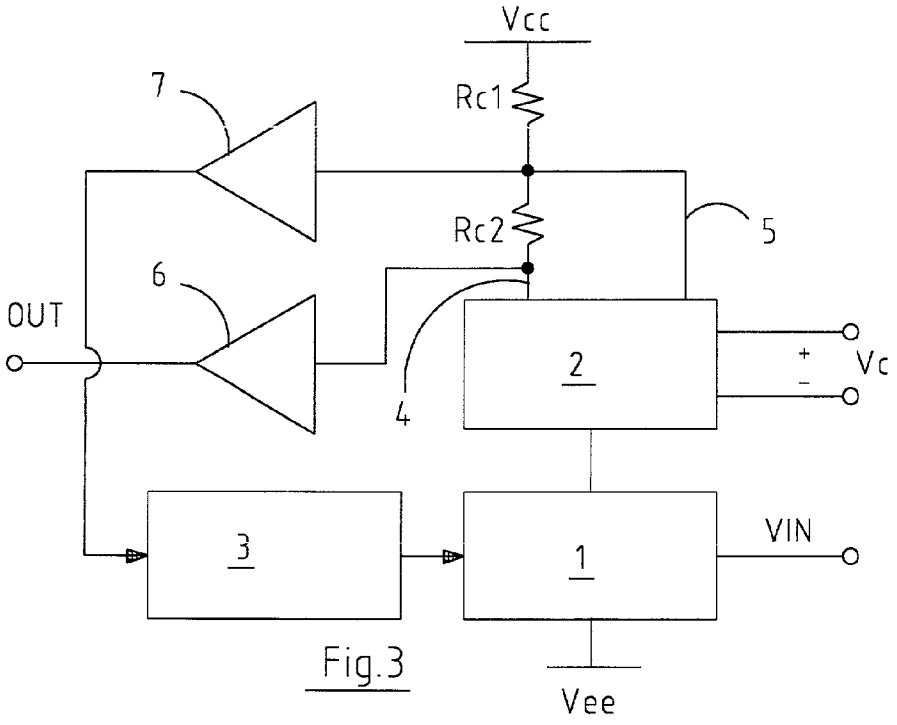

Vcc
Rc1
7
Rc2
5
6
OUT
2
+
Vc
-
4
3
1
VIN
Vee

Fig.3

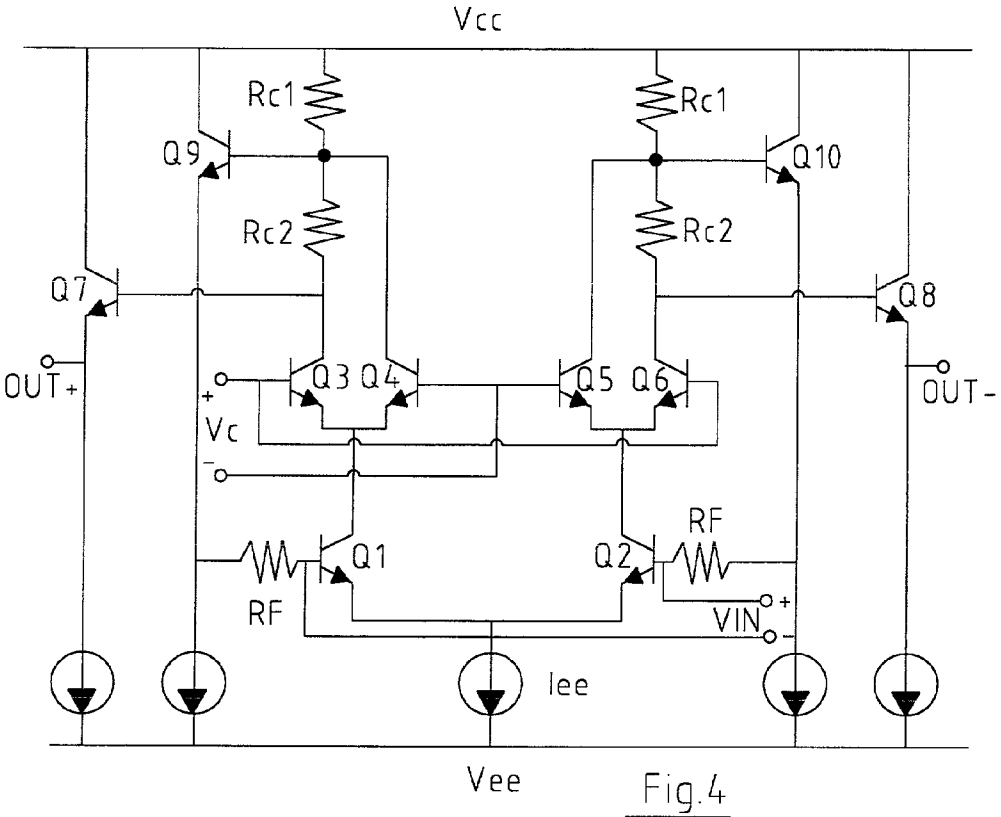

Vcc
Rc1
Rc1
Q9
Q10
Rc2
Rc2
Q7
Q8
OUT+
Q3 Q4
Q5 Q6
OUT-
+
Vc
-
RF
Q1
Q2
RF
VIN
+
-
Iee
Vee

Fig.4

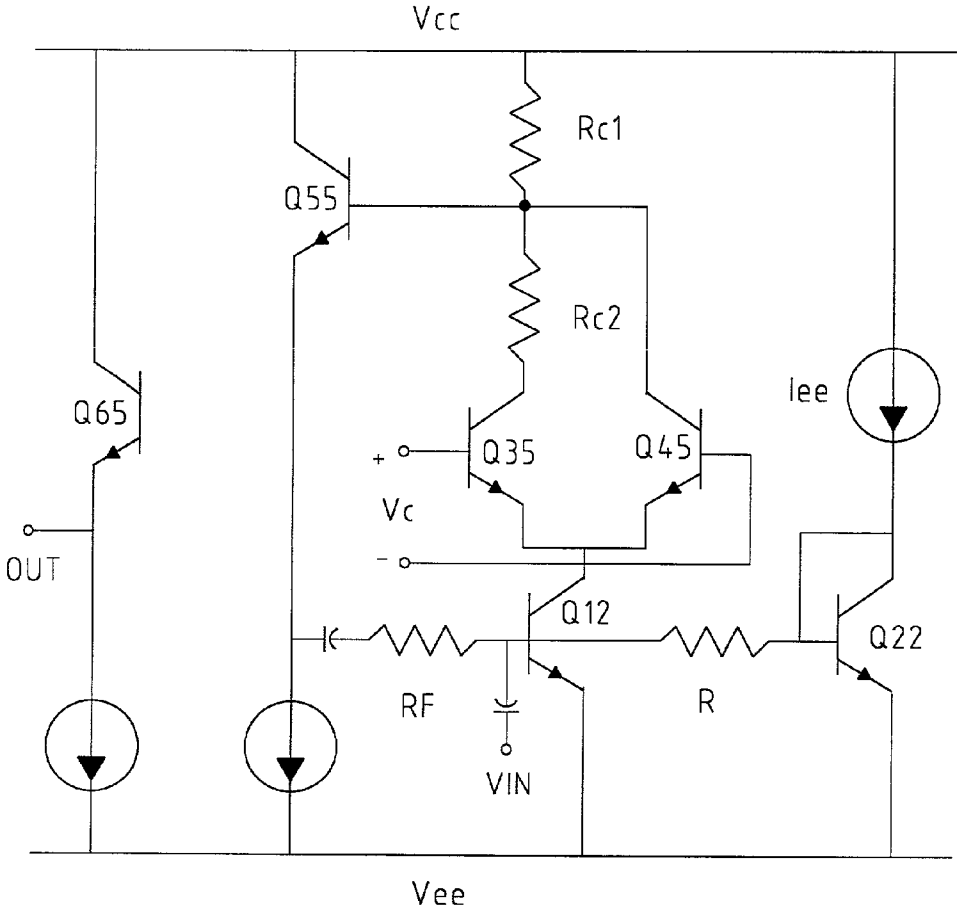


Fig.5

LOW NOISE AMPLIFIER

[0001] The present invention refers to a low noise amplifier, particularly to a radio frequency low noise amplifier.

[0002] In the field of telecommunication integrated devices a low noise amplifier is typically utilized as input stage for a receiver. Such amplifiers must assure besides a low noise in working frequency band thereof, even an efficient reduction of the distortion of the signals that are to be amplified.

[0003] Many problems of the same circuit of the amplifier are linked both to the optimisation of the noise and distortion performances and the control of the input impedance of the amplifier. Such problems have, above all in the radio frequency field, a basilar importance because the input impedance of the amplifier fixes, with a given source resistor, the adaptation conditions of the amplifier circuit at its interface with the input signal, thereby causing the ROS (Stationary Wave Ratio) of the receiver.

[0004] Open loop or feedback technologies can be utilized to control the input impedance of the low noise amplifiers. A typical circuit typology of a low noise amplifier that uses a feedback technology is shown in **FIG. 1** where a differential stage is described which is constituted by two bipolar transistors Q**10** and Q**20** which have the emitter terminals connected with each other and with a current generator lee, connected in turn with the voltage Vee, and the respective collector terminals connected with each emitter terminal of two bipolar transistors Q**30** and Q**40**. Such transistors have each base terminal connected with a bias voltage VB and each collector terminal connected both with a resistor Rc, connected in turn with a supply voltage Vcc, and with a base terminal of the transistors Q**50** and Q**60** which have in turn the collector terminals connected with the supply voltage Vcc and the emitter terminals connected with current generators connected with the voltage Vee. The base terminals of the transistors Q**10** and Q**20**, which represent the input terminals of the amplifier (which has in input a voltage VIN), are coupled with the emitter terminals of the transistors Q**50** and Q**60**, which represent the output terminals OUT− and OUT+ of the amplifier, by means of a resistor RF. In such amplifier the input impedance is fixed by the feedback resistor RF and it is equal to:

$$Ri \approx \frac{2RF}{Av} = \frac{2RF}{g_{m1,2}Rc}$$

[0005] wherein Av is the voltage gain of the amplifier circuit. Since the input impedance in such circuit configuration of the amplifier is fixed by a physical resistor and by a voltage gain, it results constant in a very large frequency band and therefore it makes this circuit configuration adapted to the large band appliances.

[0006] However a circuit configuration as that in **FIG. 1** does not allow to solve the distortion problem. An added specification required to a low noise amplifier is therefore the gain variability, in fact an adjustable gain allows to optimise the distortion performances of the amplifier. The gain variation can be controlled statically by a regulation with an external trimming or a software programming, or it can be controlled by means of a closed loop technology with an AGC (Automatic Gain Control) circuit. An amplifier employing a technology of the above mentioned type is shown in **FIG. 2** where a differential stage is shown which is constituted by two bipolar transistors Q**11** and Q**21** the emitter terminals of which are connected with each other and with a current generator lee, connected in turn with the voltage Vee, and the respective collector terminals connected with other two differential stages Q**31**, Q**41** and Q**51**, Q**61** and specifically with their emitter terminals. The collector terminals of the transistors Q**31** and Q**51** are connected with a resistor Rc, connected in turn with a supply voltage Vcc, and with a base terminal of the transistor Q**70**, while the collector terminals of the transistors Q**41** and Q**61** are connected with a resistor Rc, connected in turn with the supply voltage Vcc, and with the base terminal of the transistor Q**80**. The collector terminals of the transistors Q**70** and Q**80** are connected with the supply voltage Vcc while each one of the emitter terminals, which constitute respectively the output terminals OUT− and OUT+, is connected with a current generator connected with the voltage Vee. The base terminals of the transistors Q**11** and Q**21** constitute the input terminals of the amplifier (which has in input a voltage VIN), while between the common base terminal of the transistors Q**41** and Q**51** and the common base terminal of the transistors Q**31** and Q**61** a voltage Vc is applied which serves to regulate the gain of the low noise amplifier. By such a circuit configuration a maximum gain is obtained equal to:

$$Av_{MAX}=g_{m1,2}Rc$$

[0007] for example with a voltage Vc≧0.2V, while the minimum gain is obtained for example with Vc=0 and it is limited only by the incorrect coupling (mismatch) of the transistor couples belonging to the three differential stages.

[0008] However in such circuit configuration the input impedance cannot be correctly controlled; in fact the insertion of the variable gain does not allows to achieve a constant input impedance.

[0009] In view of the art described, it is an object of the present invention to provide a low noise amplifier that overcomes the aforementioned problem.

[0010] According to the present invention, such object is obtained by means of a low noise amplifier comprising a first circuit block suitable for converting a first amplifier input voltage signal into current, a second circuit block adapted to divide the current coming from said first block, said second block being controlled by a second voltage signal, said first and second blocks conferring a variable voltage gain to the amplifier, characterised by comprising at least one first and at least one second resistors and a feedback network said at least one first resistor connected with one first output terminal of said second block and with a supply voltage, and said at least one second resistor being connected between said at least one first and at least one second output terminals of said second block, and said feedback network being coupled with said at least one first terminal and with said first circuit block, and said at least one second terminal being coupled with at least one output terminal of said low noise amplifier.

[0011] Thanks to the present invention it is possible to provide a low noise amplifier having the variable gain and fixed input impedance features.

[0012] The features and the advantages of the present invention will be made evident by the following detailed description of a particular embodiment thereof, illustrated as not limiting example in the annexed drawings, wherein:

[0013] **FIG. 1** is a circuit scheme of a first radio frequency low noise amplifier according to the prior art;

[0014] **FIG. 2** is a circuit scheme of a second radio frequency low noise amplifier according to the prior art;

[0015] **FIG. 3** is a circuit scheme of a radio frequency low noise amplifier according to the invention;

[0016] **FIG. 4** is a more detailed circuit scheme of the amplifier in **FIG. 3** according to a first embodiment of the present invention;

[0017] **FIG. 5** is a more detailed circuit scheme of the amplifier in **FIG. 3** according to a variant of the embodiment in **FIG. 4**.

[0018] In **FIG. 3 a** circuit scheme of a radio frequency low noise amplifier according to invention is shown which comprises a voltage/current converter **1**, which has in input a voltage VIN and which is connected with a voltage Vee and with a block **2** constituted by a current divider controlled by a voltage Vc. The block **1** and the block **2** give to the amplifier a variable voltage gain. The block **2** has two output terminals **4** and **5** which are connected respectively the first one with a terminal of a resistor Rc**2** and the second one both with the other terminal of the resistor Rc**2** and with a resistor Rc**1** connected with the supply voltage Vcc. The output terminal **4** is connected with a buffer **6** the output of which represents the output OUT of the amplifier, while the second terminal **5** is connected with a buffer **7** the output of which is connected with a feedback network **3** connected with the voltage/current converter **1**.

[0019] A more detailed circuit scheme of the amplifier in **FIG. 3** according to a first embodiment of the invention is shown in **FIG. 4**. The voltage/current converter is constituted by a differential stage comprising two bipolar transistors Q**1** and Q**2** which have the emitter terminals connected to each other and with a current generator Iee, connected in turn with the voltage Vee, while the base terminals are the input of the low noise amplifier. The block **2** is constituted by two differential stages Q**3**, Q**4** and Q**5**, Q**6** the emitter terminals of which are connected with collector terminals of the differential stage Q**1**, Q**2**. Each collector terminal of the transistors Q**4** and Q**5** is connected with a resistor Rc**1** having its other terminal connected with the voltage Vcc and with the resistor Rc**2** having its other terminal connected with the collector terminal of the respective transistor Q**3** or Q**6**. Each collector terminal of the transistors Q**3** and Q**6** is connected with the base terminal of respective transistors Q**7** and Q**8**, which represent the buffer **6** and have the collector terminals connected with the supply voltage Vcc and the emitter terminals, which represent the amplifier output terminals OUT+ and OUT−, connected with respective current generators connected with the voltage Vee. Each collector terminal of the transistors Q**4** and Q**5** is connected with the base terminal of respective transistors Q**9** and Q**10**, which represent the buffer **7** and have the collector terminals connected with the supply voltage Vcc and the emitter terminals connected with respective current generators connected with the voltage Vee and with the resistors RF, which represent the feedback network **3** and are connected with the base terminals of the transistors Q**1** and Q**2** which represent the input terminals of the amplifier having in input a voltage VIN. A voltage Vc, which allows to regulate the gain of the low noise amplifier, is applied between the common base terminal of the transistors Q**4** and Q**5** and the common base terminal of the transistors Q**3** and Q**6**.

[0020] In the above mentioned circuit the voltage gain Av goes from a minimum gain given by:

$$Av_{MIN} = \frac{V(OUT+) - V(OUT-)}{VIN} = g_{ml,2} Rc1$$

[0021] which is obtained when the collector currents flow respectively through Q**3** and Q**6**, for example with Vc≦−0.2V, to a maximum gain given by:

$$Av_{MAX} = \frac{V(OUT+) - V(OUT-)}{VIN} = g_{ml,2}(Rc1 + Rc2)$$

[0022] which is obtained when the collector currents flow through Q**4** and Q**5**, for example with Vc≧0.2V.

[0023] Therefore there is a voltage gain variation given by:

$$\Delta Av = Av_{MAX} - Av_{MIN} = g_{m1,2} Rc2$$

[0024] Since the whole collector current of Q**1** and Q**2** flows always through the resistors Rc**1**, the loop is closed by means of the transistors Q**9** and Q**10** with a constant loop gain given by:

$$Avloop = g_{m1,2} Rc1$$

[0025] The input impedance, which depends on the loop gain of the circuit, results thus constant and it is given by:

$$Ri \approx \frac{2RF}{Avloop} = \frac{2RF}{g_{ml,2} Rc}$$

[0026] In **FIG. 5 a** circuit scheme of a low noise amplifier according to a variant of the above mentioned embodiment is shown. The voltage/current converter **1** is constituted by a bipolar transistor Q**12** having the emitter terminal connected with the voltage Vee and the base terminal, which constitutes the input of the low noise amplifier, is connected by means of a resistor RB with a diode connected transistor Q**22** connected with the voltage Vee and with a current generator connected in turn with the supply voltage Vcc. The block **2** is constituted by a differential stage Q**35**, Q**45** the emitter terminals of which are connected with the collector terminal of the transistor Q**12**. The collector terminal of the transistor Q**45** is connected with a resistor Rc**1** having its other terminal connected with the voltage Vcc and with a resistor Rc**2** having its other terminal connected with the collector terminal of the respective transistor Q**35**. The collector terminal of the transistor Q**35** is connected with the base terminal of a transistor Q**65**, which represents the buffer **6**, that has the collector terminal connected with the supply voltage Vcc and the emitter terminal, which represents the amplifier output terminal OUT, connected with a current

generator coupled with the voltage Vee. The collector terminal of the transistor Q**45** is connected with the base terminal of a transistor Q**55**, which represents the buffer **7** and has the collector terminal connected with the supply voltage Vcc and the emitter terminal connected with a current generator connected with the voltage Vee and coupled with a resistors RF, which represent the feedback network **3** and is connected with the base terminal of the transistor Q**12** which represent the input terminal of the amplifier having in input a voltage VIN. A voltage Vc, which allows to regulate the gain of the low noise amplifier, is applied between the base terminal of the transistor Q**45** and the base terminal of the transistor Q**35**. Such single endeed circuit architecture is suitable for low voltage appliances, for example with a voltage lower than 2V.

1. Low noise amplifier comprising a first circuit block suitable for converting a first amplifier input voltage signal into current, a second circuit block adapted to divide the current coming from said first block, said second block being controlled by a second voltage signal, said first and second blocks conferring a variable voltage gain to the amplifier, characterised by comprising at least one first and at least one second resistors and a feedback network, said at least one first resistor connected with a first output terminal of said second block and with a supply voltage, and said at least one second resistor being connected between said at least one first and at least one second output terminals of said second block, and said feedback network being coupled with said at least one first terminal and with said first circuit block, and said at least one second terminal being coupled with at least one output terminal of said low noise amplifier.

2. Amplifier according to claim 1, characterized by comprising a first buffer placed between said at least one second output terminal of the second circuit block and the at least one output terminal of said amplifier, and a second buffer placed between at least one first output of the second circuit block and said feedback network.

3. Amplifier according to claim 1, characterized in that said first block comprises a first and a second transistors forming a first differential stage and the input terminals of said transistors being the input terminals of the amplifier, said second block comprises a third and a fourth transistors forming a second differential stage and a fifth and a sixth transistors forming third differential stage, said third and said sixth transistors having a first input terminal in common and said fourth and said fifth transistors having a second input terminal in common and said second voltage signal being applied between said first and said second input terminals, said amplifier comprising two first resistors and two second resistors and consequently said second block having two first output terminals and two second output terminals, one of said first output terminals being the output terminal of said fourth transistor and the other of said two first output terminals being the output terminal of said fifth transistor, one of said two second output terminals being the output terminal of said third transistor and the other of said two second output terminals being the output terminal of said sixth transistor, and said feedback network comprising two resistors each coupled with one of said two first input terminals of the second block and with one of said two respective input terminals of the first and second transistor of the first block, and said two output terminals of the second block being coupled with two respective output terminals of the amplifier.

4. Amplifier according to claim 1, characterized in that said first block comprises a first transistor the input terminal of which is coupled with the input terminal of the amplifier, in that said second block comprises a second and a third transistors forming a differential stage, said second voltage signal being applied between the input terminals of said second and said third transistors, said amplifier comprising a first and a second resistors and consequently said second block having a first and a second output terminals coincident to the respective output terminals of said third and said second transistors, said feedback network comprising a resistor coupled with said first terminal and said second terminal of the first block, and said second terminal being coupled with a respective output terminal of the amplifier.

5. Amplifier according to claims **3** or **4**, characterized in that the input terminals of said transistors are drivable terminals while the output terminals of said transistors being non-drivable terminals.

6. Amplifier according to claims **3** or **4**, characterized in that said transistors are bipolar transistors.

7. Amplifier according to claims **3** or **4**, characterized in that said transistors are MOS transistors.

8. Amplifier according to claims **3** or **4**, characterized in that said transistors are biCMOS transistors.

9. Amplifier according to claims **3** or **4**, characterized by comprising current generators suitable for biasing said transistors.

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