S16-2 A Full Color AC Plasma Display with 256 Gray Scale

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ABSTRACT

The practical 256 gray scale technology for an ac plasma panel has been developed through the A D S sub-field method and the newly introduced low voltage addressing technology. Performance of a 21 inch full color plasma panel with 640x3 480 line and the integrated electronics using monolithic drivers will be presented.

INTRODUCTION

Plasma displays have been expected as the most suitable display device for a large size direct-view wall hanging HDTV because of its simple processes which is suitable for making a large panel,its good display quality as self-emitting type, it quick response, and so on.

In recent years, many valuable works have been reported in dc and ac panels(1). As to dc panels, a full color TV display with 256 gray scale has been demonstrated utilizing the Pulse Memory Driving Technology(2).

On the other hand, ac panels are on delivery already on a commercial basis with a 21 inch three color display for a stock-exchange transaction, thanks to the inherent features of long life and high luminance(3). However, a high gray level technology has not yet been made until now. The highest achievement of gray levels of ac plasma panel was 64 levels (4) and this is why a higher level gray scale technologies are being looking forward to for a long time.

In the last symposium of SID('92), Fujitsu proposed the new technology of "ADS sub-field method (Address Display period Separated sub-field method) which has a potential of achieving the 256 gray scales, and showed the 31 inch diagonal full color plasma panel with 64 gray scale(5).

The authors have developed an ac full color plasma display with 256 gray scale, using the above A D S sub-field method incorporating with newly introduced addressing technology. This paper describes the driving technology, electronics and the performance obtained.

SPECIFICATION OF THE PLASMA PANEL

Table 1 shows the specification of the panel. A 21 inch in diagonal surface discharge type with 640 × 480 pixels(=1920×480 subpixels) was used. The RGB color subpixels are arranged in a straight line by trio basis as shown in table 1. The subpixel pitch is 0.22 mm, and resulting horizontal and vertical pitch of pixel is 0.66 mm respectively. Principles are the same as the 31 inch panel reported at SID '92 (5).

The panel structure is illustrated in figure 1. The front glass substrate bears two set of parallel sustain electrodes (X and Y). These electrodes are composed of transparent electrodes and auxiliary electrodes. The auxiliary electrode which prevents from voltage drop due to resistance of transparent electrode is formed on the transparent electrode. These are covered by a dielectric layer. The separators (barrier ribs) are formed on the dielectric layer perpendicular to sustain electrodes in order to isolate the discharge coupling between adjacent cells. These are covered by a MgO layer. On the other substrate, address electrodes are formed. The separators are formed between address electrodes. Three color phosphors (R,G,B) are deposited over the address electrode. All components except sustain electrodes and a MgO layer are composed by thick film printing method. Gap between two substrate are about 100 um and a Ne+Xe gas mixture is filled in this space.

Table 1 Specification of Experimental Panel

	Specification
Display Area	21in. (422.4mm×316.8mm)
Number of Pixels	640 × 480
Number of Subpixels	1920× 480
Pixel pitch	0.66 mm
Subpixel pitch	0.22 mm(H)× 0.66 mm(v)
Subpixel arrangement	RGBRGB

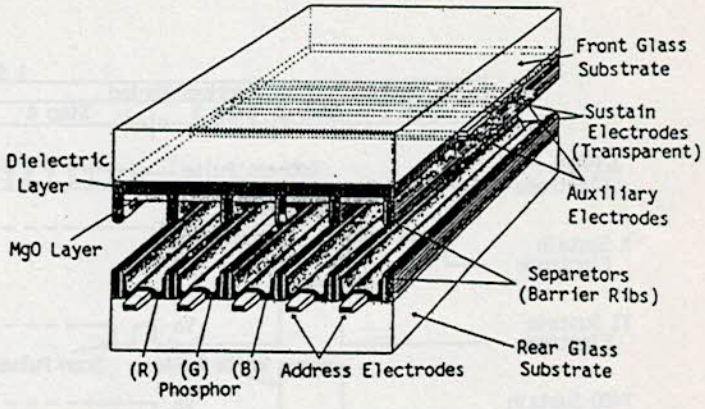

Fig.1 Panel structure

DRIVING TECHNOLOGY

Figure 2 explaines the driving sequence for 256 gray scale display using the technology of the Address Display period Separated sub-field method(5). The frame is divided into 8 subfield in each of which the address period and the sustain period are separated. In the address period, the wall charges are formed preliminary in the pixels corresponding to the whole screen at first. And then sustain pulses are applied to whole screen to display. The number of sustain pulse is changed corresponding to the brightness of the sub-field. This driving technology proposed in last SID('92) enables a high speed operation of addressing, which promises 256 gray scale. And it has another advantage of reducing the sustain frequency, accordingly the power consumption of sustain pulses has been reduced drastically.

While, in the practical 256 gray scale display, the higher address frequency more than 200 kHz is required. Then, the low voltage addressing technology is indispensable to suppress the power consumption. In the conventional addressing method using self-erase discharge mechanism, following problems still remained. In order to execute the self-erase discharge, it is necessary to make a lot of wall charges. Therefore high addressing voltage is required, that so large electronical power is consumed, under the driving condition of 256 gray scale. And consequently, the power reduction and the integration of the electronics were limited.

In order to solve the problems, the authors have developed a low voltage addressing method.

Addressing is performed by the newly developed procedure as follows.

(1)Whole-screen erasing
(2)Whole-screen writing
(3)Whole-screen erasing
(4)and Sequential addressing by writing into display line.

--- 3us * 480 lines ---

Figure 3 shows the driving waveform. The whole-screen erasing of first step (1) is executed in order to make the all discharge dots into the same state without influence of last sustain period. Step(2) whole-screen writing is executed between X and Y electrodes. At that instant the part of ion is stacked on the surface of the phosphors by address electrodes maintained 0V. In step(3), the extra wall charge is erased. This erase pulse can be modeled as mechanism of wide erase pulse, s the wall charges remains after discharge. Last step(4) is sequential addressing by writing into display line. The address discharge between Y and address electrodes can be ignited with the extremely low voltage. Because ions are stacked on a phosphor and electrons are stacked on MgO layer upper Y electrode. These charges functions effectively.

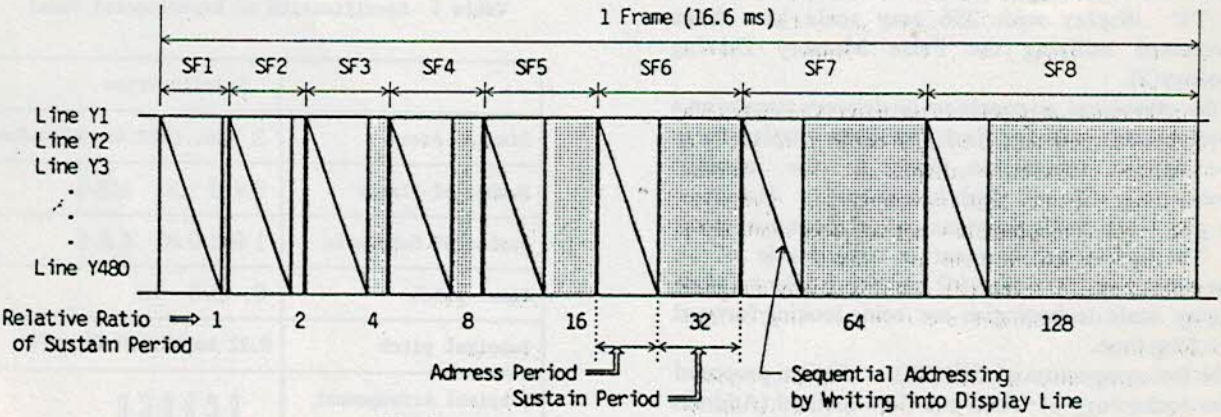

Fig.2 Driving sequence for 256 gray scale
(A D S sub-fileld method)

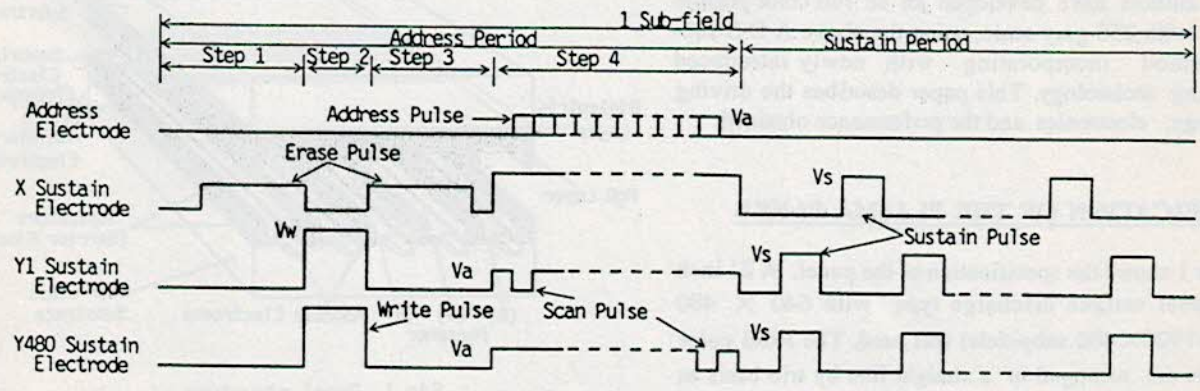

Fig.3 Driving waveform

This introduction of the above sequence has enabled the low voltage and high speed operation. Figure 4 shows the characteristic of dynamic margin, under the driving condition of 3 us address cycle time per a line. The address voltage is reduced to 50V from 80V of the former 31 inch panel which utilized a conventional address method of whole-write/selective-erase addressing by self-erase discharge. The period of sustain cycle is 8 us and its width is 3.5 us.

The frame is divided into 8 of sub-fields each of which has the binary graded brightness , for example,the brightness of the first subfield SF1 to be B0, SF2 to be 2 × B0 ,,, the 8th SF8 to be 128 × B0, as shown in figure 2. Each sub-field is formed by addres speriod and sustain period. Each address period takes 1.5 ms, then the accumulated time for one frame takes 12 ms. The residual 4 ms of the frame period is assigned for sustain period. The total of 510 sustain cycles can be generated and assigned into 8 sub-fields, sustain cycle of the first subfield SF1 to be 2 cycles, SF2 to be 4 cycles ,,, the 8th SF8 to be 256 cycles . The average sustain frequency of 30kHz is obtained.

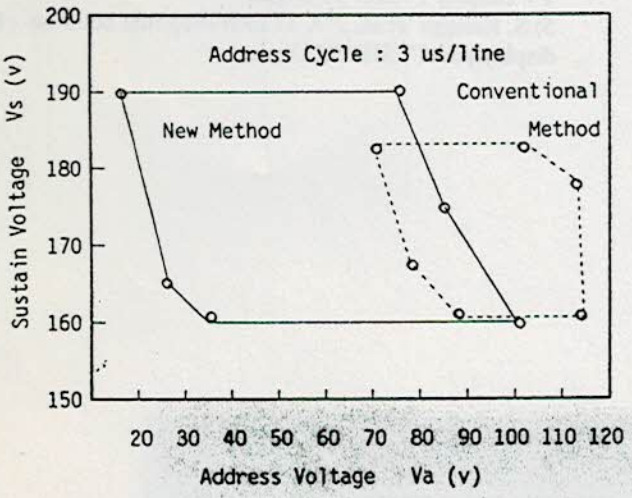

Fig.4 Characteristic of dynamic margin

ELECTRONICS

In order to realize the practical display system using the above technology, the drivers and controllers must be integrated. Two kinds of 64 bit monolithic drivers of 100 pin QFP are developed as the address and the scan drivers. The controller is integrated into 3 chips of gate arrays, except for the part of frame memories.

Figure 5 shows a block diagram of the driving electronics. It is configured with drivers, controller and DCDC converter for subsidiary voltage sources, and integrated compactly on single printed wired board.

The driving circuitry is formed with common sustain pulser for X and Y, and the monolithic drivers mentioned above. The address drivers are used in the manner of direct-drive to address electrodes, however, scan drivers are superimposed on the Y sustain pulser in the manner of floating-drive. The control signals for the scan drivers are fed by photocouplers.

The control circuitry includes three gate arrays and frame memories. Three kinds of 8 bit brightness data for R, G and B are stored temporarily into the frame memories, then transmitted to address drivers in correspondence with the address operations. The signals for scan drivers are also generated and transmitted synchronously. In this way, the gatearrays control the memories and execute the generation of all the drivers' signals.

The sources required for this unit are only two voltages ; Vs for sustaining and Vcc for logic, utilizing DCDC converters mentioned above.

PERFORMANCE

Table 2 explaines the performance of the experimentally fabricated unit. The full color display with 256 gray scale has been achieved. The area average luminance of "white" was 200 cd/m2, which is the highest level ever reported and sufficient for practical use. A photograph of the 21-in. full color display is presented in figure 6.

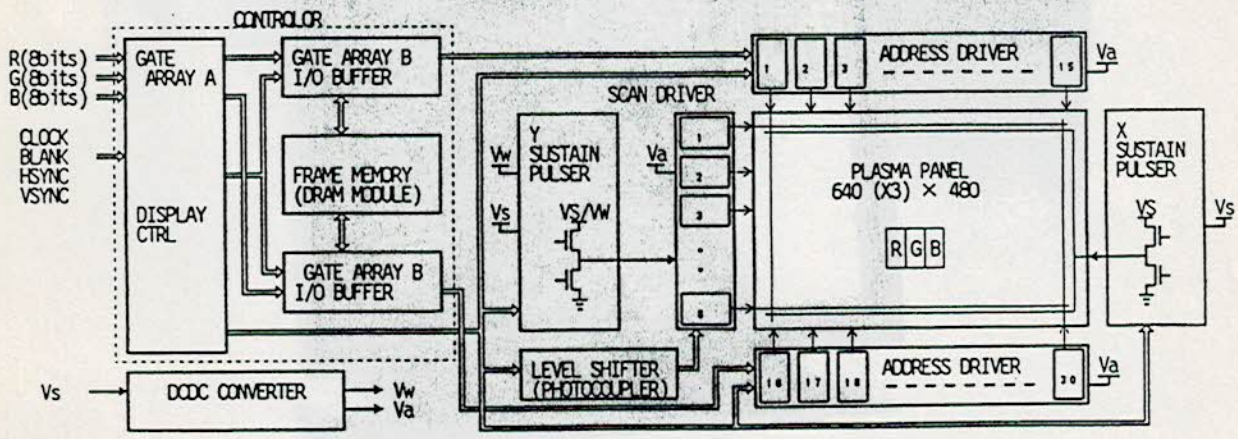

Fig.5 Block diagram of the driving electronics

Table 2. Performance of the Experimentally Fabricated Unit

		Performance
Display capacity (Number of cells)		640 × 480 (1920 ×480)
Gray level		256 (16.7 million colors)
Area Luminance		200 cd/m² (white) -- 30kHz --
Contrast		~50 : 1
Power consumption		100 W TYP.
Power Source	Vs	180 V
	Vcc	5 V

CONCLUSION

The impact of this paper is as follows:

Utilizing the A D S sub-field method and the new addressing method are proposed here,

(1) the 256 gray scale in ac plasma panel has been realized, with

(2) the monolithic display drivers.

Furthermore, the high luminance of 200 cd/m² was obtained. It can be said by these achievements that ac color plasma display has reached to the stage of practical use for conventional TV's or multi-media display PCs as an engine.

The authors believe that the ac plasma has made an effective step for realizing HDTV in the size of 40 to 60 inches.

ACKNOWLEDGMENTS

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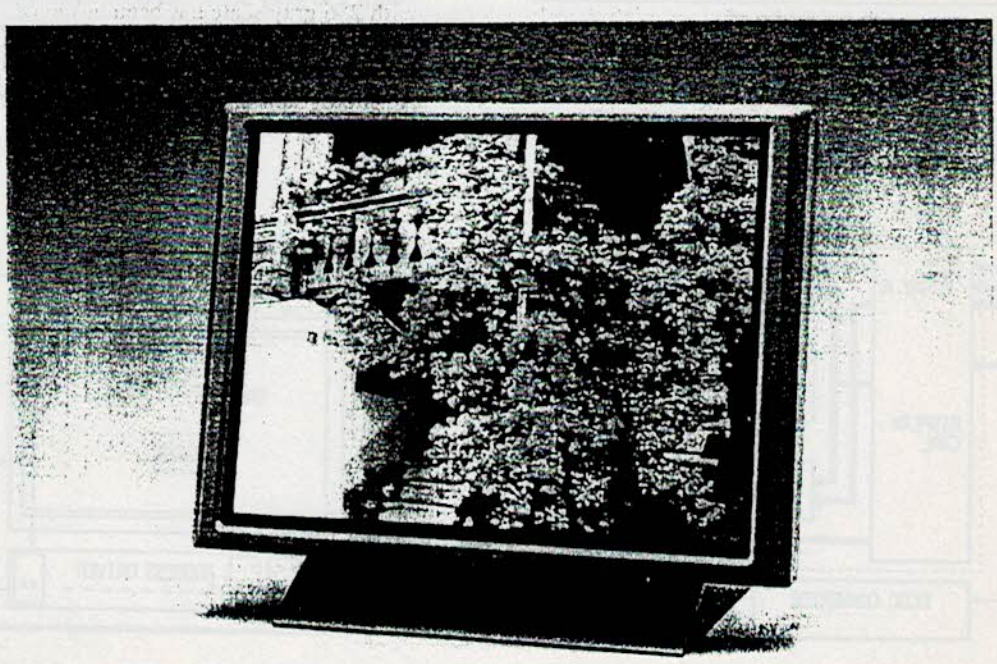

Fig.6 Photograph of 21-in. full color display