Single chip DMT–modem transceiver for ADSL

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Abstract — The complete digital processing of the Discrete Multitone modulation technique has been integrated into a single device, processed in 0.5u standard CMOS. The optimal power and area result (realized by algorithmic optimisations) and the extended programmability make this component the basis to build cost effective ADSL systems.

I. Introduction

Asymmetric Digital Subscriber Line (ADSL) is intended to provide multi–megabit per second digital signals to the customer over the unconditioned twisted pair telephone network (see fig. 1). A return channel (from customer premises to the local exchange) at a much lower rate is also provided for control and request of downstream information. ADSL offers the important advantage to multiplex this digital information above a conventional analog voice channel. So, customers subscribing to analog POTS service can maintain that service while having access to the ADSL digital services. With ADSL, applications such as Video on Demand (VOD) or fast internet access become feasable on the unconditioned twisted pair.

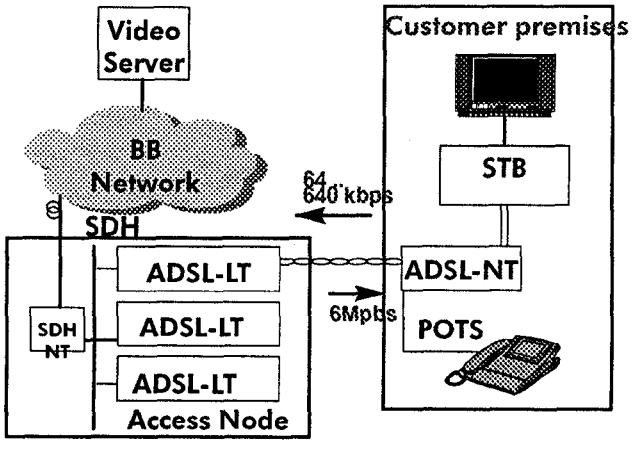

Fig.1: ADSL system overview

The modulation technique for ADSL, which has been standardised in T1.143, is Discrete Multi–Tone (DMT). DMT modulation is a special form of multicarrier modulation ([1],[2]). Fundamentally, DMT modulation superimposes several carrier–modulated waveforms to represent the input bit stream. The DMT transmit signal (see fig. 2) is the sum of N independent sub–signals, each of equal bandwidth and equispaced with center frequency f_i, i = 1, ..., N. Each of these sub–channels can be considered to be Quadrature Amplitude Modulated (QAM) signal. In DMT modulation, the number of bits of input data that are allocated to the distinct sub–channels is variable : sub–channels that will encounter less attenuation and less noise will carry more bits of information.

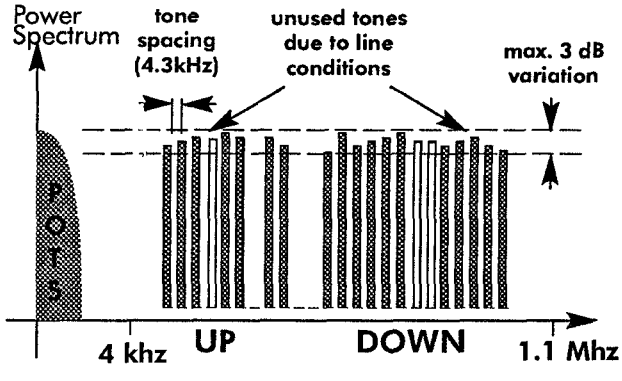

Fig. 2: DMT Spectrum

The ADSL concept has been proposed at the beginning of the decade [3]. Since then, several manufacturers have embarked on an ADSL development. The chip we propose reaches the highest integration level. The complete digital processing for the ADSL modem functionality is integrated in the single device called DACHA (Digital signal and CHannel processor for ADSL).

II. Architecture

The DACHA is used in both central office and remote applications, and is designed for sampling rates up to 4.4MHz, with DMT symbols at 4 kHz and 2.2 MHz sampling. The clock frequency used by the DACHA for internal digital signal processing is 36 MHz.

Inside DACHA, the recieve and transmit parts are fully seperated (see fig. 3). In the transmit direction, a Forward Error Correction Code is implemented to deal with both random errors and impulse noise on the line. The Reed Solomon is ful-

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ly programmable : the overhead bytes can be any number between 2 and 32, the wordlenght can be up to 255. The interleaving depth can range from 2 till 64. A convolutional interleaving scheme is implemented as the more area efficient solution. Both the interleave and the deinterleave RAM are integrated, so that no external components are required. The protected digital bitstream is mapped onto DMT carriers.
In the IFFT module, first a rotor and gain correction are applied in the frequency domain. Then a frequency to time domain conversion is executed with an IFFT algorithm. This architecture is elaborated further in the next section.

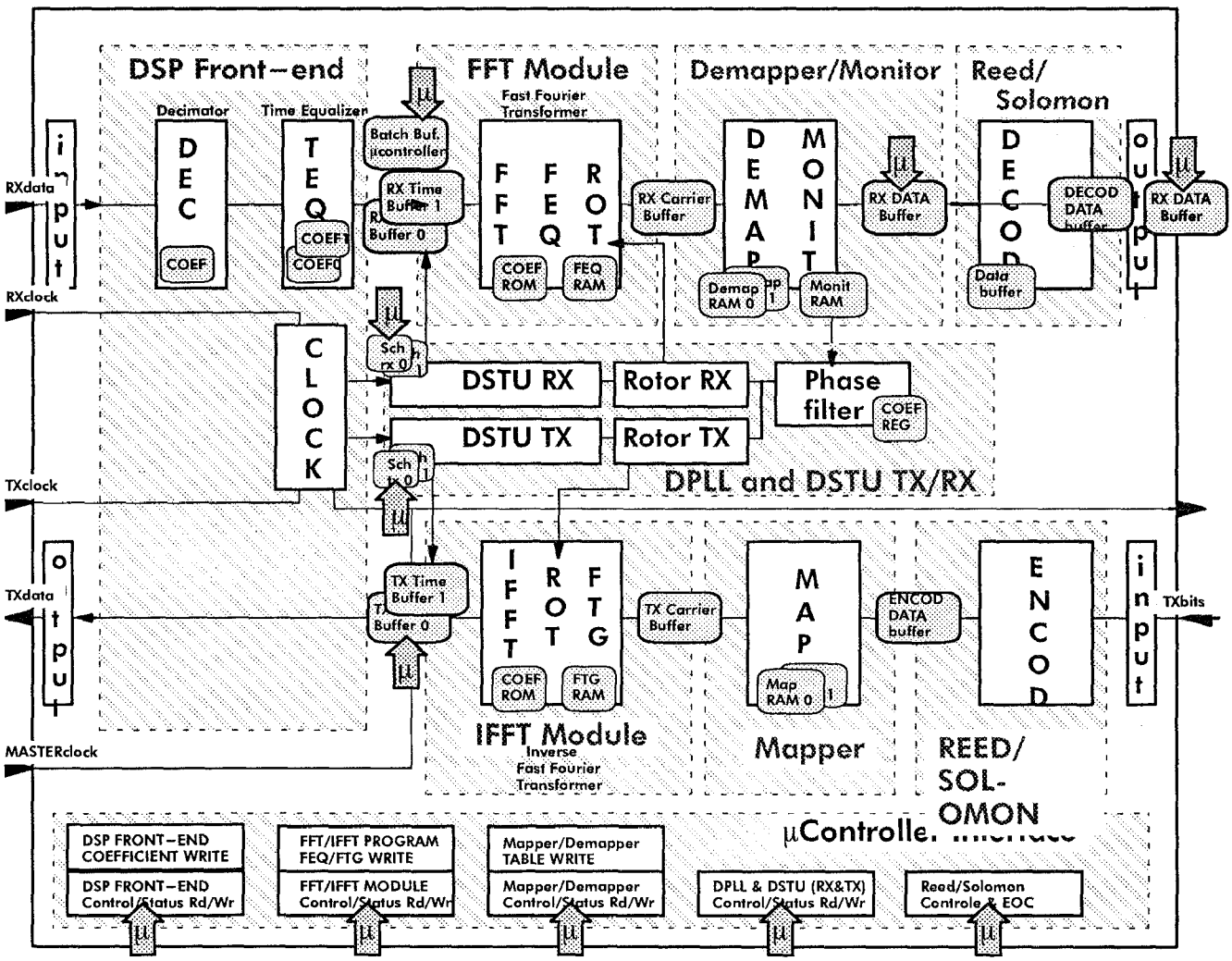

Fig. 3: Chip architecture

The complementary functions are performed in the receive direction. In the DSP front end, the rx–signal is decimated from 4.4 MHz to 2.2 MHz and equalized in the time domain. This fucntionality is implemented by FIR filters.
In the FFT module, the signal is first converted from the time domain to the frequency domain. In the frequency domain, a rotor and equalizing step are executed.
The DMT carriers are demapped to a digital bit stream. The error and noise is monitored on individual carriers and on pilot tones.
Random errors and erasures are corrected in the Reed Solomon decoding, burst errors are corrected with deinterleaving.

III. Timing and Control

Control and clock recovery is a crucial element in every modem design. In DACHA, a hierarchical approach has been adopted for the control functions which guarantees the optimal performance/flexibility mix.

The tracking of the pilot tone is a very fast control function, so this lowest level of control is fully implemented in HW. The pilot phase deviations are accumulated and filtered, which yields the rotor phase. This rotor phase is used to rotate the received carriers, which is equivalent to a time

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domain interpollation : a rotation of 90 degrees for the highest 1.1 MHz carrier corresponds to a shift of half a sample at 2.2 MHz. When the rotor has grown to 180 degrees (on the sampling frequency), one RX period is deleted from or added to the DMT RX sampling clock and an adjustment of a complete time sample is realized. This way, a time base of the RX data is maintained : position of samples within a symbol, symbols between synchronisation symbols, guard time length, etc.
Also the total Δf between the incoming data and the local Xtal is measured. This information is passed via a dedicated output directly to the VCXO, or is read via the bus by the micro–controller, which can use the information to update the external VCXO.

One level higher in the control hierarchy, the different slave peripherals have to be activated to do all processing for each DMT symbol : (I)FFT, (de)mapper, Reed–Solomon encoding/decoding, (de)interleaving. For every step in the initialisation sequence, the moments within the DMT symbol when the slave modules have to be activated and the parameters with which they have to be called, are different. At particular times within the initialisation sequence, also single events have to be induced : TEQ and decimator coefficient list swap, (de)mapper table swap, monitor table swaps, etc. Therefor, this timing module is conceived as a flexible machine with programmable tables. These scheduling tables can be configured to change the state of a number of control lines (which activate the slave modules) at programmable times.

At the highest level, the DACHA is controlled and configured by an external processor. All coefficients, parameters, tables, slave module programs are loaded by the controller. The ADSL initialisation sequence is also under external control.

This programmable architecture allows a lot of flexibility. Different algorithms can be implemented and evaluated, to select the optimal one, and all that with the same HW device.

IV. Fast Fourier Transform, including Rotor, FEQ and FTG

The Fast Fourier Transformer is instantiated twice in the DACHA. It is used as DMT carrier demodulator in the RX direction and as modulator in the TX direction. It is a dedicated programmable machine, which can do all processing for one DMT symbol in less than 250 us (see fig. 4). It has a 70 MMult/s performance, and is based on a dedicated pipelined multiplier–accumulator ALU.

The ALU contains 2 20x18 fixed point multipliers and two busses : one for data (which is 20 + 20 = 40 bits wide) and one for coefficients (18 + 18 = 36 bits wide). The ALU performs the following 8 basic operations.

– complex radix–4 decimation in time (I)FFT butterfly
– complex radix–2 decimation in time (I)FFT butterfly
– special 'resolve' butterfly to combine the split results of four real FFTs
– final radix–4 butterfly after the resolve butterfly to present positive frequency results only.
– special first radix–2 decimation in frequency IFFT butterfly, from positive frequency components only.
– special resolve butterfly to combine the results of the special first DIF butterfly to a complex input for a complex IFFT.
– complex times complex multiplication, plus 2^N scaling.
– complex times real multiplication.
A programming module (controlled by the external micro–processor) which runs in the (I)FFT module, combines these basic operations, so that all correct operations in every initialisation step can be executed. This flexibility allows for future algorithm optimisations.

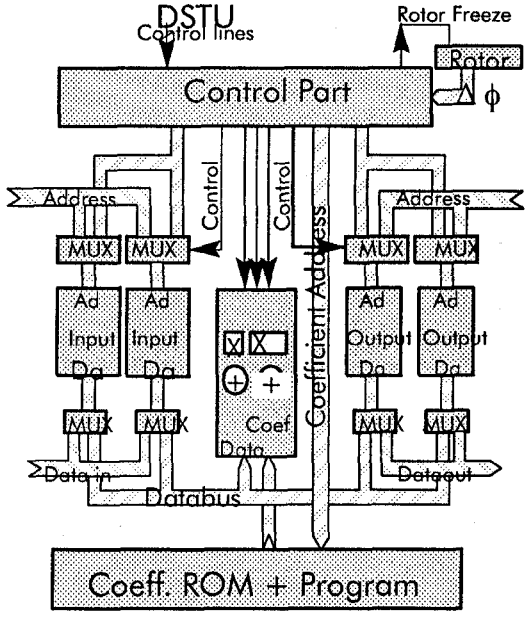

Fig. 4: FFT architecture

In the RX direction, the Fast Fourier Transformer is used as DMT carrier demodulator. It performs the following RX functions :
– A real time to positive frequencies FFT, from 512 time samples to 256 complex positive frequencies. This requires a number of CFFT scans (1 radix–2 and 3 radix–4), one special complex to positive freequencies resolve scan, and a last radix–4 scan. This special algorithm can be used due to the fact that the input is a real time sequence. This reduces the processing requirements by a factor of 2, resulting in a major complexity reduction so that a single chip solution becomes feasable.
– The FEQ (frequency equalisation) is a rotation to allign the received carriers on the demapper X and Y axis, plus a fine

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gain, normally between 0 and –6 dB. the scaling step (which is combined with the FEQ) is an extra scalar multiplication with 2^N to boost the gain of the weakest carreirs with K . 6dB.
– The FFT module does then a ROTOR calculation of all positive frequencies. This is a linear phase correction, which compensates a misallignment of the sampling clock. Actually it interpolates the sampling clock of the received data to any intermediate point, but in the frequency domain. The following formula applies :

$$f_i = f_i \cdot e^{j.2\Pi \cdot i \cdot \Delta\Phi} \quad (1)$$

where $i \cdot \Delta\Phi$ is the content of an accumulator, incremented with $\Delta\Phi$ for each next frequency.
– The previous actions are performed in about 150 usec. This leaves sufficient spare time to do extra DSP functions in 'off–line' or 'batch' processing for the micro–controller. This allows the controller to be rather simple in the remote location, while in the central office, the controller can be shared by 4 ADSL lines. This allows a major system cost reduction.

In the TX direction, the complementary operations are performed : rotor calculation (to adjust the frequency error between the local X–tal and the desired TX frequency), fine tune gain (correcting gain of the individual carriers) and IFFT from positive frequencies to real time (with the same factor of 2 reduction in processing power as in RX direction). On top of that, also an interpollation step is included. The straightforward way to do this is to add an FIR filter after the default IFFT (which transforms 256 complex frequencies to 512 time samples). However, the better way is to extend the input sequence with 256 zeroes and to perform a 512 complex frequencies to 1024 time samples IFFT. This can be realized in the available 250 usec and is more area efficient. Indeed, the complexity of the IFFT grows only with N.logN (requiring only 1 extra multiplier), while for an extra FIR filter at least 2 multipliers would be required.

V. Results

The device (see fig. 6) has an overall complexity of 250 Kgates. Also 320 kbits of RAM are integrated, most of which is allocated by the (de)interleave RAMs. The chip is processed in a 0.5u standard CMOS process, and has an area of 160 mm2. The worst case power consumption is 1.6 W and the device is packaged in a 144 PQFP package with heat spreader.
Silicon of the device is available and the component has proven full functionality in a stand–alone test (after a metal change). The FFT shows an accuracy of 90 dB. The pilot tracking has been measured to be stable within 3 degrees (see fig. 5) which guarantees the stability of the system.
The system integration of the device is ongoing, with optimisation of the TEQ and FEQ algorithms to reach the maximum performance.

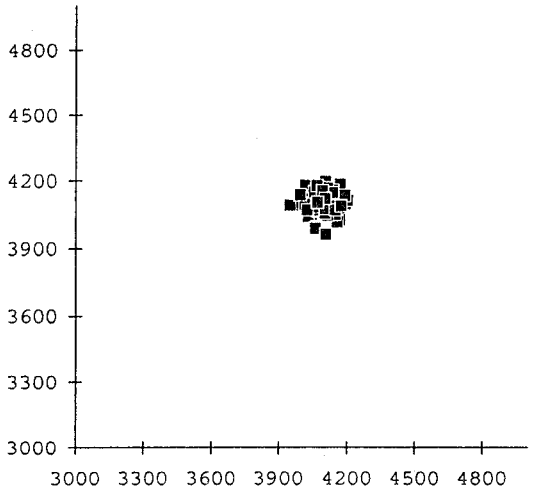

Fig. 5: Pilot tracking diagram

VI. Conclusion

A single chip digital DMT modem transceiver for ADSL applications has been realized. The device is processed in a 0.5u standard CMOS technology. Algorithmic optimisation of the core (I)FFT functionality have lead to an optimal power and area result. The extended programmability opportunities make this device the cornerstone for future ADSL systems in development.

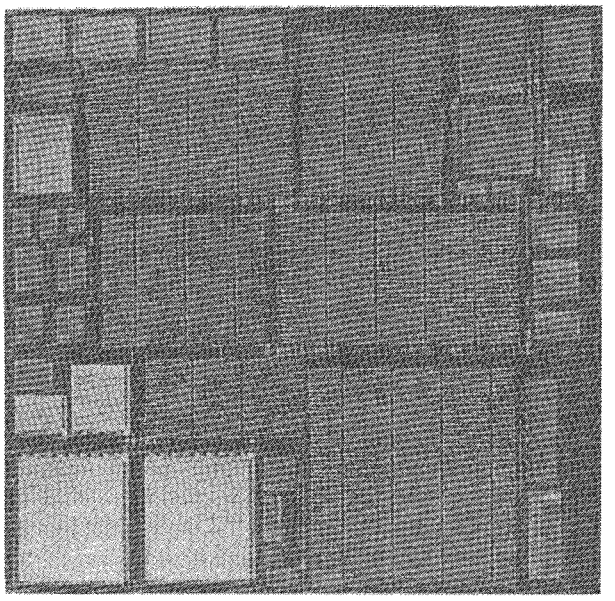
Fig.6: Photograph

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