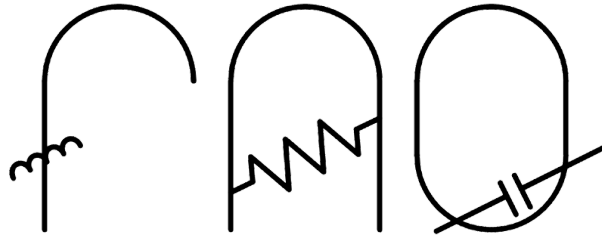


# ELECTRONICS

SEARCH



*THE HOWS AND WHYS OF  
ELECTRONICS*

## Inside a WorldSpace satellite radio receiver

January 29, 2014

**W** is no longer

operational. But I had  
a receiver lying around  
from when it was  
active. I opened it up  
and here is what I  
found in it:

Labels

*Under the hood*



Antenna Unit



Front Panel

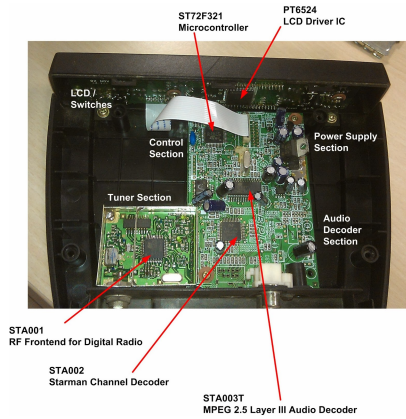


Inside of the front

panel



Main Board



Mainboard with the various sections marked out

**STA001 – RF Frontend for Digital Radio**

- Single chip receiver for

satellite digital

transmission

- Superheterodyne

receiver with IF

output

- High input

intercept point,

low Mixer noise

- 54db IF VGA gain

range

- Adjustable RF

gain

- Adjustable IF gain

- Integrated RF

VCO

- Integrated IF

VCO

- Integrated

synthesizer

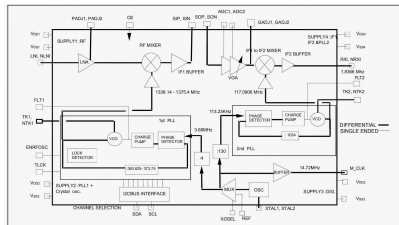
- I<sup>2</sup>C bus

compatible

programming

Interface

- Unregulated 2.7 volts to 3.3 volts voltage Supply
- Low cost external components



## Block Diagram of STA001 – RF Frontend for Digital Radio

---

## STA002 – Starman Channel Decoder

- Front end interface
  - IF input carrier frequency:  $f = 1.84 \text{ MHz}$
  - Single internal 6 bit

A/D

converter

- QPSK

demodulation

n

- Input symbol

frequency:  $F_s$

= 1.84

Msymbols/s

- Digital

Nyquist root

filter:

- Roll-off

value of

0.4

- Digital

carrier loop:

- On-chip

quadrature

demodulation

and tracking

loop

loop

loop

- lock detector
- C/N indicator
- Digital timing

recovery:

- Internal timing error evaluation, filter and correction

- Digital AGC:

- Internal signal power estimation and filter
- Output control signal for AGC (1 bit

PWM)

- Forward error correction
  - Inner decoder
    - Viterbi soft decoder for convolutional codes, constraint length  $M=7$ , Rate  $1/2$
  - Deinterleave r block
  - Outer decoder
    - Reed-Solomon decoder for 32



parity  
bytes;  
correcti  
on of up  
to 16  
byte  
errors

- Block  
lengths:

255

- Energy  
dispersal  
descram  
bler

- Back end

Interface

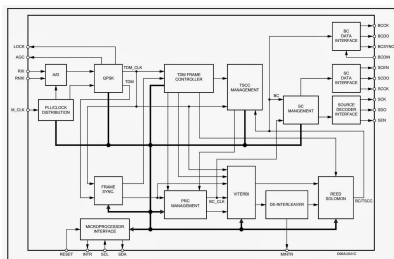
- Broadcast

Channel  
selection

- Audio

Service  
Component  
selection to  
MPEG

- decoder
  - Service Component selection
  - Control
    - I<sup>2</sup>C serial Bus control interface
  - Decryption
    - WES Scheme



Block Diagram  
of STA002 – Starman  
Channel Decoder

---

## STA003T – MPEG 2.5

### Layer III Audio

### Decoder

- Single chip  
MPEG2 layer 3

decoder

- Supporting
  - 
  - All features specified for Layer III in ISO/IEC 11172-3 (MPEG 1 Audio) except 44.1KHz Audio
  - All features specified for Layer III 2 channels in ISO/IEC13818-3.2 (MPEG 2 Audio) except 22.05KHz Audio
  - Lower sampling

frequencies  
syntax  
extension,  
(not specified  
by ISO) called  
MPEG 2.5  
except  
11.025KHz  
Audio

- Decodes layer III  
stereo channels,  
dual channel,  
single channel  
(mono)
- Supporting the  
MPEG 1 & 2  
sampling  
frequencies and  
the extension to  
MPEG 2.5:  
48, 32, 24, 16, 12,  
8 kHz
- Accepts MPEG  
2.5 layer III

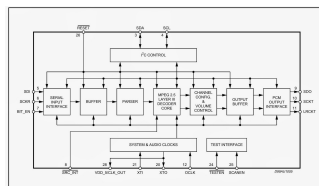
elementary  
compressed  
bitstream with  
data rate from 8  
kbit/s up to 128  
kbit/s

- Digital volume control
  
- Digital bass & treble control
- Serial bitstream input interface
- Ancillary data extraction via I<sup>2</sup>C interface.
- Serial PCM output interface (I<sup>2</sup>S and other formats)
- PLL for internal clock and for output PCM clock generation

- Low power data elaboration for power consumption optimisation
- CRC check and synchronisation error detection

with software indicators

- I<sup>2</sup>C control bus
- Low power 3.3 volts CMOS technology
- 14.72 MHz external input clock or built-in crystal oscillator



Block Diagram  
of STA003T –  
MPEG 2.5 Layer

## III Audio Decoder

---

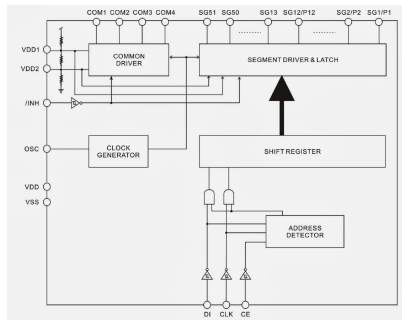
### PT6524 - LCD Driver

#### IC

- CMOS  
Technology
- Up to 4 Common  
and 51 Segment  
Drivers
- Up to 204 LCD  
Segments
- Up to 12 General  
Purpose Output  
Ports
- 1/4 Duty - 1/2  
Bias or 1/4 Duty -  
1/3 Bias Drive  
Technique
- No Decoder  
Intervention  
Necessary to  
Display the Data
- Power Saving

Mode provided

- RC Oscillation  
Circuit



Block Diagram

of PT6524 – LCD  
Driver IC

---

**ST72F321 –**

**Microcontroller**

- Memories
  - 32K to 60K  
dual voltage  
High Density  
Flash  
(HDFlash) or  
ROM with  
read-out  
protection



capability. In-  
Application  
Programming  
and In-  
Circuit  
Programming  
for HDFlash  
devices

- 1K to 2K  
RAM
- HDFlash  
endurance:  
100 cycles,  
data  
retention: 20  
years at 55°C
- Clock, Reset And  
Supply  
Management
  - Enhanced  
low voltage  
supervisor  
(LVD) for

main supply  
and auxiliary  
voltage  
detector  
(AVD) with  
interrupt  
capability

- Clock  
sources:  
  
crystal/ceram  
ic resonator  
oscillators,  
internal RC  
oscillator,  
clock security  
system and  
bypass for  
external  
clock

- PLL for 2x  
frequency  
multiplicatio  
n

- Four Power

Saving

Modes: Halt,

Active-Halt,

Wait and

Slow

- Interrupt

Management

- Nested  
interrupt

controller

- 14 interrupt  
vectors plus  
TRAP and  
RESET

- Top Level  
Interrupt  
(TLI) pin on  
64-pin  
devices

- 15 external  
interrupt  
lines (on 4  
vectors)

- Up to 48 I/O Ports

- 48/32  
multifunction  
al  
bidirectional  
I/O lines
- 34/22  
alternate  
function lines
  
- 16/12 high  
sink outputs
- 5 Timers
  - Main Clock  
Controller  
with: Real  
time base,
  - Beep and  
Clock-out  
capabilities
  - Configurable  
watchdog  
timer
  - Two 16-bit  
timers with: 2

input

captures, 2

output

compares,

external

clock input

on one timer,

PWM and

pulse

generator

modes

- o 8-bit PWM

Auto-reload

timer with: 2

input

captures, 4

PWM

outputs,

output

compare and

time base

interrupt,

external

clock with

event

detector

- 3

Communications

Interfaces

- SPI

synchronous

serial

interface

- SCI

asynchronou

s serial

interface

- I<sup>2</sup>C multimas

ter interface

- 1 Analog

peripherals

- 10-bit ADC

with up to 16

input ports

- Instruction Set

- 8-bit Data

Manipulation

- 63 Basic



# Block Diagram of ST72F321 - Microcontroller

**LABELS:**

UNDER THE HOOD

**SHARE**

Comments



**Kanwar Brara**

· January 31, 2014 at  
1:08 PM

have you found a way to reprogram it? ive been trying to find anything related to it on the web but have failed. on the normal broadcast you get yazmi audio.....which is playing old maestro channel tunes.....any ideas?~?

**REPLY**



**Anurag Chugh**

· January 31, 2014 at  
5:08 PM

Hi,  
I broke my WorldSpace opening it :P. So of course it won't work any more.



Meanwhile try the  
Saregama  
Workspace app for  
Android:  
<https://play.google.com/store/apps/details?id=com.srgm.activities&hl=en> it seems  
to have the Farishta  
Channel too!!

### REPLY

**Anonymous**

· April 15, 2014 at  
1:52 PM

dear Anurag  
I also own a tongshi  
damb-r receiver,  
that i dismantle, i  
found inside a tuner  
labelled TDW-A  
(200509 05)  
Have you got  
information about  
this tuner, or could  
you tell me if yours  
device features a  
usb port for linking  
to a pc computer in  
order to receive  
data.  
FYI Worldspace  
satellite still  
operational with a  
US company called  
omni-sat  
Waiting for your  
reply.  
thanks

### REPLY



Anurag Chugh



· April 15, 2014 at  
2:49 PM

Hi, I am not aware  
of the TDW part  
number. My device  
does not have a  
USB Port

**REPLY**



**Unknown**  
· June 8, 2014 at  
7:21 PM

Hai all ...i want used  
world space  
satellite radio and

antenna (or  
antenna)

**REPLY**

To leave a comment, click  
the button below to sign  
in with Google.



About Me



**Anurag Chugh**  
Pune, Maharashtra, India

## VISIT PROFILE

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Archive 

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Labels 

 Powered by Blogger