DOLBY AC-3™ and MPEG-2 AUDIO DECODER IC WITH 6-CHANNELS OUTPUT

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Dolby AC-3 and MPEG-2 are two different standards for the compression of up to 6 independent digital audio channels into a single serial bit stream. This paper describes a DSP-based integrated circuit which implements the two decoding algorithms, allowing to recover the original pulse code modulation (PCM) information from the encoded bit stream. It describes also the methodology which was employed to design and validate the software embedded on the chip.

INTRODUCTION

Consumer applications such as digital television (including HDTV), DVD (digital video disc) and multimedia will provide up to 6 independent audio channels (conventional stereo + centre, surround and subwoofer channels) for high quality audio reproduction. To solve the problem of storage and transmission of these 6 independent channels, some algorithms have been developed to compress the signals in a single digital bitstream : Dolby AC-3 and the ISO standard MPEG-2 Audio (for multichannel reproduction). The paper describes an integrated circuit which is able to decode in real time the 6 audio signals simultaneously from a bit stream encoded with one of the two algorithms. The first section describes the general features of the circuit, then a description of the internal chip architecture is given, and then we focus on the methodology employed to design and validate simultaneously the DSP architecture and the software running on it.

GENERAL FEATURES

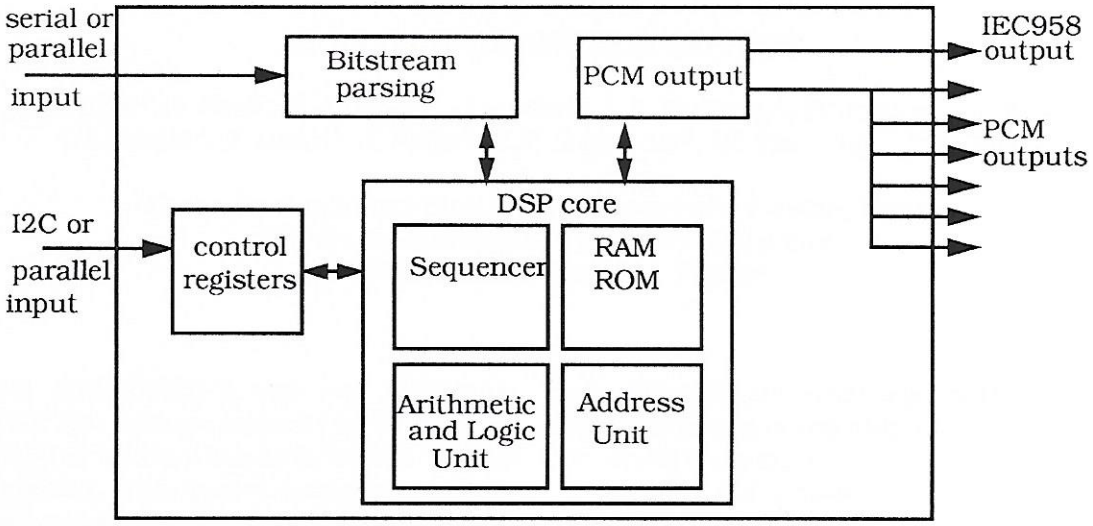
The chip is able to decode either Dolby AC-3 or MPEG2 Audio coded bitstreams, carrying up to 6 independent channels. In addition, it includes a Dolby Pro Logic decoder and a bass redirection algorithm for the subwoofer output.
The interfaces of the chip are :

- serial data input
- parallel data input
- ADC input
- parallel control interface
- I2C control interface
- three standard PCM (Pulse Code Modulation) outputs carrying 2 channels each
- IEC 958 output

The chip is working with a 33 Mhz internal clock.

CHIP ARCHITECTURE

The chip is composed of a DSP core surrounded by hardware blocks in charge of bitstream synchronization and PCM output.
The DSP core is a VLIW (Very Long Instruction Word) machine optimized for audio applications, working on 24 bits data. It includes an ALU (Arithmetic and Logic Unit) including a shifter, multiplier and accumulator, allowing to perform classical signal processing algorithms efficiently. An address unit allows to have several addressing modes, including modulo and bit-reverse addressing (for FFT-like algorithms). The program flow is controlled by the sequencer, which allows fast hardware loop mechanism and interrupt handling.
Program and data are located in separate memories, allowing to perform most operations in one cycle. The DSP core is highly orthogonal, allowing the execution of many operations in parallel. The DSP core is controlling (via the software) several hardware blocks which are in charge of extracting data from the incoming bitstream (finding synchronization words) and providing PCM-decoded data to the outputs. These blocks are programmable by the software, and interact with the DSP core with interrupts. They work in parallel with the program being executed on the DSP core, allowing decoding in real time with a limited clock frequency.



DESIGN METHODOLOGY

Architecture choices

Because of the high level of complexity of the two algorithms, and because they were still changing when we started to implement the decoder, it was chosen a DSP-based approach to adapt easily to necessary changes.

Hardware design

All the hardware has been described either in VHDL or in schematic, and simulated separately with the appropriate CAD tool. As there is no "intelligence" in the hardware blocks outside the DSP core (no complex state machine), the design of these blocks has been quite fast. The DSP core itself has been customized for the two algorithms, using specific hardware for multiply-accumulate operations and addressing modes.

Software design and co-validation

The software for Dolby AC-3, MPEG-2 multichannel audio and Dolby Pro-Logic has been written in C language. The validation of the software on the DSP hardware has been done as follows:

- execution of the algorithms on Unix workstation (using standard Unix C compiler), and comparison with a reference decoder,
- compilation for the DSP core with the use of an efficient compiler adapted to the architecture,
- simulation of the binary code on a cycle-accurate simulator of the DSP. This simulator has been written in C and is a perfect model of the DSP, which allows to simulate the chip very quickly. The simulation time is very much shorter than the simulation time of a gate-level simulator working on a netlist, because there are no propagation time calculations.
- a final simulation is made on the real netlist with a gate-level simulator.

The use of the cycle-accurate simulator has allowed to validate easily the decoding software on the DSP. As it is very closed to the real implementation, it was also useful to validate the hardware, and to prove that the system was working in real time. It has been the key factor for a fast validation and development of the chip, and has allowed to correct most of hardware and software bugs, leading to a robust solution.

CONCLUSION

A DSP-based architecture surrounded by specific hardware blocks was chosen for its efficiency, and the methodology employed (co-validation of software and hardware with the help of a cycle-accurate simulator) has allowed to design this decoder in a very short time. It has been placed and routed in 0.5 micron CMOS technology and manufactured, and was fully functional at the first silicon. The chip is now in production.

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Note : Dolby AC-3 and Dolby Pro Logic are trademarks of Dolby Laboratories Licensing Corporation.