IEEE Milestone Proposal:
"Creating the Foundation for the Data Storage Flash Memory Industry"

Plaque Wording

"System Flash," a flash memory chip architecture that is coupled to a dedicated controller and firmware to manage the memory cells so as to emulate a magnetic disk, was pioneered by Eli Harari and SanDisk. This architecture's evolution from NOR to multistate NAND flash enabled a new class of portable computing devices by displacing photographic film and magnetic and optical media, allowing ubiquitous access to personal data.

(bronze plaque to be placed in the Visitors' Lobby in Bldg. 6
at SanDisk Headquarters in Milpitas, CA)

Abstract

Flash memory used for mass data storage has supplanted the photographic film and floppy disk markets. It has also largely replaced the use of magnetic tape, CD, DVD and magnetic hard disk drives (HDDs). This usage of Flash Memory has grown into a $25 billion industry in the past 20 years by enabling digital cameras, MP3 players, smart phones and tablet PCs. Flash data storage allows for numerous read and write/erase cycles, many years of data retention and high density at low cost. This technology's stringent requirements were successfully achieved by applying Fowler-Nordheim tunneling through ~70 Angstrom (Å) tunnel oxide and sophisticated programming schemes. The vision for Flash in mass data storage applications was incubated in the mid-70s following studies of wear-out mechanisms in thin films of SiO_2. A complementary system level approach was then developed to provide a self-correcting, highly managed memory which emulated an HDD, and which allowed for its use as an HDD replacement. The underlying force that drove the ubiquitous use of Flash memory in consumer electronics and mobile devices has been the phenomenal cumulative cost reductions that were achieved by combining the scalability of NAND flash with multi-bit cell storage. This has allowed advances in NAND Flash memory to outpace Moore's Law.

Invention of Fowler-Nordheim Electrical-Erasable-Programmable-Read-Only-Memory (FN EEPROM) [Refs. 1, 2, 3]

Non-volatile memory was in its infancy in the early 1970s, and was mainly used for the storage of executable program code. Study of the thermal oxide conduction and charge trapping mechanisms in Eli Harari's Ph.D. thesis *Charge Trapping Effects in Thin Films of Al_2O_3 and SiO_2* in 1973 [Ref. 1] led to a future understanding of the adjustments needed for non-volatile memory to become suitable for data storage applications.

The first ultra-violet-erasable floating gate EPROM was invented by Frohman Benchkowski at Intel in 1970, and it used a gate oxide at a range of 1000 Å. By exploring much thinner SiO_2 films in the 100 Å range at Hughes Microelectronics, Harari showed that, under high electric field conditions, electron conduction through these films was an efficient and reliable mechanism for both program and erase. The responsible phenomenon was indirect tunneling from the silicon conduction band to the SiO_2 conduction band, a quantum mechanical effect known as Fowler-Nordheim Tunneling, which was first discovered by Fowler and Nordheim many years earlier. This mode of conduction was important because 100 Å films of SiO_2 would support long-term retention of electrons trapped on a floating gate. This is in sharp contrast to the 25-30 Å films of SiO_2 that were employed in those days in MNOS/SONOS for direct tunneling of electrons from the silicon conduction band into interface traps, but which were generally unreliable and incapable of long-term retention of trapped electrons.

Not much was known in 1975 about SiO_2 films in the 100 Å thickness range. These films were thought to be unreliable, and suffered from leakage and dielectric breakdown under high electric field. Harari's work at Hughes showed that SiO_2 films in the 100 Å thickness range could be thermally grown with high quality, and were highly reliable as insulators. Furthermore, when high electric fields were applied across these films, they exhibited excellent electron conduction. However, they consistently exhibited catastrophic breakdown after a certain amount of charge was passed through them. It was shown that this was intrinsic oxide breakdown, unrelated to pinholes or other imperfections or contamination. Breakdown was invariably induced by electrons trapped in cumulatively generated new oxide traps under sufficiently high applied field conditions.

A new experimental technique was than developed to characterize and optimize these thin SiO_2 films. Applying constant current conditions, two key parameters were then established: T_{BD}, the time to breakdown under given constant current conditions; and ΔV_{BD}, the voltage shift V_{FB} required to maintain the current constant up until breakdown, and which is representative of the cumulative trapped charge, Q_{BD}, at the onset of breakdown. This seminal work was published by the American Institute of Physics in its *Journal of Applied Physics* (JAP) in 1978 [Ref. 2].

These findings led directly to the development at Hughes of the first practical floating gate EEPROM, as published in US Patent 4,115,914, priority date March 26, 1976, issued Sept. 26, 1978, titled "Electrically Erasable Non-Volatile Semiconductor Memory" [Ref. 3]. This development relied on a thin SiO_2 layer to permit writing and erasing of floating gates through Fowler-Nordheim tunneling under appropriate voltage conditions applied between control gate and substrate.

In 1984, Toshiba's Masuoka invented Flash EEPROM, a simplified version of the floating gate EEPROM. In 1987, Masuoka followed up with the invention of NAND Flash, an architectural arrangement of memory cells which proved highly scalable. Now twenty-five years later, this invention still relies on SiO_2 films in the thickness range of 70-85 Å to read, write and erase each NAND cell through the very same Fowler-Nordheim tunneling mechanism.

Enabling High Reliability and High Density Flash Memory for Data Storage [Refs. 4, 5]

US patent 5,095,344, filed June, 8, 1988, issued Mar. 10, 1992, titled "Highly Compact EPROM and Flash EEPROM devices" [Ref. 4], taught a Flash EEPROM having a very high storage density (each cell storing more than one bit of information) and a long life (adaptive program and erase voltages to minimize oxide stress during cycling), "making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems."

US Patent 5,172,338, priority date April 13, 1989, issued Dec. 15, 1992, titled "Multi-state EEPROM Read and Write Circuits and Techniques" [Ref. 5], taught massively parallel programming of flash cells by applying stepped programming to designated multilevels while inhibiting further programming from correctly verified cells. These massively parallel program-inhibit circuit techniques became particularly powerful for overcoming write-speed bottlenecks. Without these techniques, practical multistate NAND (2, 3 and 4 bits-per-cell) would not be possible today. Multistate NAND is commonly known as MLC (Multi-Level Cell), as opposed to the one bit-per-cell SLC (Single-Level Cell).

System Flash [Ref. 6]

US patent 5,297,148, priority date April 13, 1989, issued Mar. 22, 1994, titled "Flash EEPROM System" [Ref. 6], teaches "[a] system of Flash memory chips with controlling circuits [that] serves as a non-volatile memory such as that provided by magnetic disk drives," one of whose characteristics is the "ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defective cells becomes large, the whole sector is remapped." This invention represented a radically new concept which is called "system Flash," characterized by a new Flash memory chip architecture working cooperatively with a dedicated intelligent hardware/firmware controller.

The rationale was the need to overcome Flash memory's inherently unreliable nature in order to create an abstraction that made it appear to the user as a 100 percent reliable technology. This was accomplished through the use of a closed-loop controller to constantly monitor and repair the Flash memory arrays for the entire operating lifetime of the storage device.

A key feature of the '148 patent was a new physical partitioning of the flash memory arrays in a manner that resembled that of HDDs. Flash memory cells were arranged together in erasable sectors, with each sector having a partition dedicated to storing user data, and a "header" partition for use solely by the controller for managing all of the Flash memory cells and sectors. The resultant abstraction provided a logical-to-physical mapping to keep track of the ever-changing file addresses and links needed to manage the Flash memory cells.

A Complete Flash System Solution

SanDisk's strategy was to develop and sell complete Flash system solutions consisting of proprietary Flash memory chips with physical sectors and headers, managed by a dedicated intelligent controller which emulated an HDD, and which was optimized for storing data and content rather than executable program code. The controller's role included the following:

- format the memory arrays,
- randomly access sectors and headers,
- implement on-the-fly ECC,
- apply dynamic defect management,
- enhance Flash system endurance by minimizing program/erase voltages based on the device's life cycle,
- level out the wear-out by tracking sector level "hot count,"
- write and verify multilevel cells,
- provide programmable reference cells, and
- numerous other proprietary tricks.

The controller also provided file management and a standard I/O interface that rendered it plug-and-play compatible with, for example, IDE HDDs. A major side benefit was that SanDisk's frequent introduction of new generations of Flash memory, including transitioning from single-bit cells to multi-bit cells, was easily accommodated by controller firmware changes that were transparent to the user.

Moore's Law Applied to Flash Scaling [Ref. 7]

Low cost is the most important requirement for mass consumer markets to take off. Moore's Law as applied to Flash scaling was executed and surpassed in the introduction of 17 new generations of flash technology over the past 21 years, with each generation doubling the number of memory bits per chip. Cost reductions were accelerated through the successful commercialization of 2 bits-per-cell (X2) and 3 bits-per-cell (X3) MLC technology. Today the vast majority of NAND flash memory bits sold by all suppliers relies on SanDisk's patented X2

and X3 technology. MLC has thus played an important role in NAND's cumulative 50,000X cost and price reductions between 1991 and 2012 [Ref. 7].

Abandoning NOR, Adopting NAND

In 1998-1999 it became clear that NOR was reaching its scaling limits and that NAND was the most attractive candidate for further scaling and cost reduction as needed for data storage. SanDisk partnered with Toshiba, the original NAND inventor, to implement a successful cooperation of NAND Flash using SanDisk's MLC knowhow. The first jointly developed 1Gb NAND MLC chip was introduced in 2002. The doubling of data density continued almost every year thereafter, along with wide acceptance of MLC by the entire industry.

NAND Flash was initially considered to be a niche technology. It was serial, with very limited applications that included voice recorders. However, NAND proved to be ideally suited for data storage applications primarily because of its inherently superior scalability. This scalability came primarily from two factors. First, it offered highly regular memory arrays with highly efficient contacts and therefore almost a cross-point 4F2 cell. Second, it relied on highly efficient, extremely low current Fowler-Nordheim tunneling for both write and erase. This combination allowed the implementation of massive parallelisms in write and erase operations – a dramatic improvement in performance compared to NOR flash – and yet was easy on battery life for portable applications. NAND Flash is by far the dominant flash storage technology. The NAND Flash market quickly embraced MLC, which today represents approximately 90 percent of the NAND bits shipped.

Conclusion

NAND's ability to emulate an HDD within System Flash, along with the cost benefit of MLC, has enabled new classes of devices and a sophistication that simply would not have been possible otherwise. Storage of data in Flash Memory, including digital content, has allowed access to digital photography and cell phones in portable products used in all walks of life worldwide. Ubiquitous access to personal data is now a reality.

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Ref #	Date and Location	Reference Type	Reference Title	Significance	Applicable Excerpt
1	**1973; Princeton, NJ**	Princeton Univ. Ph.D. Thesis of Eli Harari	**"Charge Trapping Effects in Thin Films of Al_2O_3 and SiO_2"**	Study of thermal oxide conduction and charge trapping effects led to the future understanding of thin SiO_2 films later used in floating-gate EEPROM and Flash EEPROM	
2	**1978; Hughes Aircraft, Newport Beach, CA and Irvine, CA**	Journal of Applied Physics (JAP) paper	**"Dielectric breakdown in electrically stressed thin films of thermal SiO_2"**	A novel technique enables many program/erase cycles and long data retention as needed for data storage application.	"A novel technique is described which was used to study the intrinsic breakdown mechanism in films of thermal SiO_2 in the thickness range of 30-300 Å. It was determined that high-field and high electron injection current conditions existing in the films just prior to breakdown result in the generation of a very high density of defects which behave electrically as stable electron traps. … [T]he breakdown mechanism is intimately related to the rate of generation of the electron traps." (Abstract)
3	**Priority Date: 1976, Issued: 1978; Hughes Aircraft, Newport Beach, CA and Irvine, CA**	US Patent 4,115,914	**"Electrically Erasable Non-Volatile semiconductor Memory"**	First practical Floating Gate EEPROM, teaching the use of Fowler Nordheim tunneling through relatively thin films of SiO_2 to rapidly program and erase a floating gate transistor while enabling long data retention and high endurance. This mechanism is used in all modern day NAND Flash	"The general purpose of this invention is to provide a new and improved non-volatile field effect memory structure and the fabrication process therefor, having most if not all, of the advantages and features of similarly employed devices and related processes, while eliminating many of the aforementioned disadvantages of prior art structures." (3:10-16)

Ref #	Date and Location	Reference Type	Reference Title	Significance	Applicable Excerpt
4	**Filed: 1988, Issued: 1992; Los Altos, CA**	US Patent 5,095,344	**"Highly Compact EPROM and Flash EEPROM devices"**	Flash EEPROM having a very high storage density (each cell storing more than one bit of information) and a long life (adaptive program and erase voltages to minimize oxide stress during cycling), "making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems." These Flash MLC and adaptive program/erase algorithms are the cornerstones of modern day flash-based SSDs, memory cards and USB sticks.	"An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems." (Abstract)
5	**Priority Date: 1989, Issued: 1992; SunDisk Corp., Santa Clara , CA and Los Gatos, CA**	US Patent 5,172,338	**"Multistate EEPROM Read and Write Circuits and Techniques"**	Massively parallel programming of flash cells by applying stepped programming to designated multilevels while inhibiting further programming from correctly verified cells. These massively parallel program-inhibit circuit techniques became particularly powerful for overcoming write-speed bottlenecks. Without these techniques, practical multistate NAND (2, 3 and 4 bits per cell) would not be possible today.	"Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells …" (Abstract)

Ref #	Date and Location	Reference Type	Reference Title	Significance	Applicable Excerpt
6	**Priority Date: 1989, Issued: 1994; SunDisk Corp., Santa Clara, CA and Los Gatos, CA**	US Patent 5,297,148	**"Flash EEPROM System"**	"A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives." (Abstract) This represented a radically new concept which was called "System Flash," and which was characterized by a new Flash memory chip architecture that worked cooperatively with a dedicated intelligent hardware/firmware controller.	"Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. … Another improvement is the ability to remap and replace defective cells with substitute cells." (Abstract)
7	**May 23, 2011; Monterey, CA**	Proceedings of 3rd IEEE International Memory Workshop (IMW)	**The Non-Volatile Memory Industry – A Personal Journey**	Eli Harari's recollections of his personal involvement as a device physicist from the early days of the non-volatile memory industry through the 22 years that he served as CEO of SanDisk Corp. (a company he co-founded in 1988).	

Dielectric breakdown in electrically stressed thin films of thermal SiO_2

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(Received 8 August 1977; accepted for publication 8 November 1977)

A novel technique is described which was used to study the intrinsic breakdown mechanism in films of thermal SiO_2 in the thickness range 30–300 Å. It was determined that high-field and high electron injection current conditions existing in the films just prior to breakdown result in the generation of a very high density of defects which behave electrically as stable electron traps. These traps are most likely generated close to the injecting electrode. The internal field in the oxide due to trapped electrons can approach 3×10^7 V/cm which appears to be the maximum field strength which Si-O bonding can withstand. At all temperatures between 77 and 393 °K, the breakdown mechanism is intimately related to the rate of generation of the electron traps. No evidence was found to support the impact ionization breakdown model. The technique is also described as a tool for yield measurements, with important implications for long-term reliability of MOS IC's.

PACS numbers: 77.50.+p, 73.60.Hy, 73.40.Qv, 72.20.Ht

I. INTRODUCTION

The rapid development of MOS technology has spurred a considerable interest in the dielectric instabilities in electrically stressed thin films of thermally grown SiO_2. This is a major reliability problem in MOS LSI and will become one of the limiting factors for maximum chip size in high-density high-performance short-channel MOS VLSI.

The majority of related work reported in the past few years[1] has dealt with large-area effects primarily related to pinholes and weak oxide spots. Because breakdown occurs first in these localized regions, their occurrence obscures phenomena associated with the intrinsic oxide breakdown mechanism. Previous researchers have, in general, relied on a self-healing breakdown technique[2–5] to isolate the intrinsic oxide breakdown from early breakdown events. The present paper describes a new technique which was used with considerable success to gain a clearer understanding of the mechanisms related to intrinsic oxide breakdown. The distinguishing feature of this new technique is that the oxide is stressed under a condition of constant oxide current, rather than constant or ramped gate voltage. This ensures a constant electric field at the charge-injecting electrode, independent of charge trapping which may occur in the oxide under the high-field conditions prevailing just prior to breakdown. Measurements were carried out on a very large number of oxide capacitors (more than 10 000 samples from many wafer lots), to ensure valid statistical data and to isolate unusual events. The effective oxide area under stress was kept very small, thereby almost completely eliminating the probability for the occurrence of early breakdowns through pinholes and other localized oxide imperfections. Oxide thicknesses examined were limited to the 30–300-Å range.

A model is proposed which qualitatively describes the mechanisms leading to intrinsic oxide breakdown. The model suggests that breakdown is closely related to the observed generation of a very high density of defects in the stressed oxide. These defects act as efficient and stable electron traps. No evidence was found to support the impact-ionization breakdown model.[6,7]

II. DEFINITION OF TERMS

Three basic parameters are used in the present study to characterize the oxide films. Each thin-oxide capacitor was stressed at a gate voltage so as to maintain a specified oxide current I. $V_{in}(I)$ is the voltage required initially on the gate to achieve an oxide current I. Under continuous electrical stress, charge is trapped in the oxide, necessitating a change in $V_{in}(I)$ in order to maintain I. $\Delta V_{BD}(I)$ is the measured change in gate voltage just prior to breakdown, i.e., $V_{BD}(I)=V_{final}(I)-V_{in}(I)$. Its magnitude is proportional to the density and spatial distribution of the charge trapped in the oxide, its sign being negative for net trapping of holes and positive for net trapping of electrons. $T_{BD}(I)$ is the measured time to breakdown at the constant current I. $+I$ denotes injection of electrons from the Si substrate into the oxide, while $-I$ denotes injection of electrons from the polysilicon gate electrode into the oxide.

III. EXPERIMENTAL PROCEDURE

A schematic of the automated test station used for data collection in these experiments is shown in Fig. 1. An HP 9830A desk calculator was programmed to control the electrical measurements, record the data, and perform statistical analysis. A digitally controlled power supply provided a prescribed constant oxide current I. The voltage required to maintain this conduction current was monitored on a DVM with a high-input-impedance op-amp buffer. The HP 9830A controlled an Electroglas semiautomatic wafer probe station, and each experiment typically involved breakdown measurements of 100–120 capacitors across the entire area of a 2-in. wafer. For each such measurement, probe contact was made with the probe at zero voltage relative to the substrate. The power supply was then ramped at a rate of 2 V/msec up to the voltage $V_{in}(I)$. With a constant current I now flowing through the oxide, the voltage was sampled at 80-msec intervals, compared with

 0021-8979/78/4904-2478$01.10

United States Patent [19]
Harari

[11] **4,115,914**
[45] **Sep. 26, 1978**

[54] **ELECTRICALLY ERASABLE NON-VOLATILE SEMICONDUCTOR MEMORY**

[75] Inventor: **Eliyahou Harari,** Irvine, Calif.

[73] Assignee: **Hughes Aircraft Company,** Culver City, Calif.

[21] Appl. No.: **770,346**

[22] Filed: **Feb. 22, 1977**

Related U.S. Application Data

[62] Division of Ser. No. 671,183, Mar. 26, 1976.

[51] **Int. Cl.**[2] **H01L 29/78**
[52] **U.S. Cl.** **29/571**
[58] **Field of Search** 29/571

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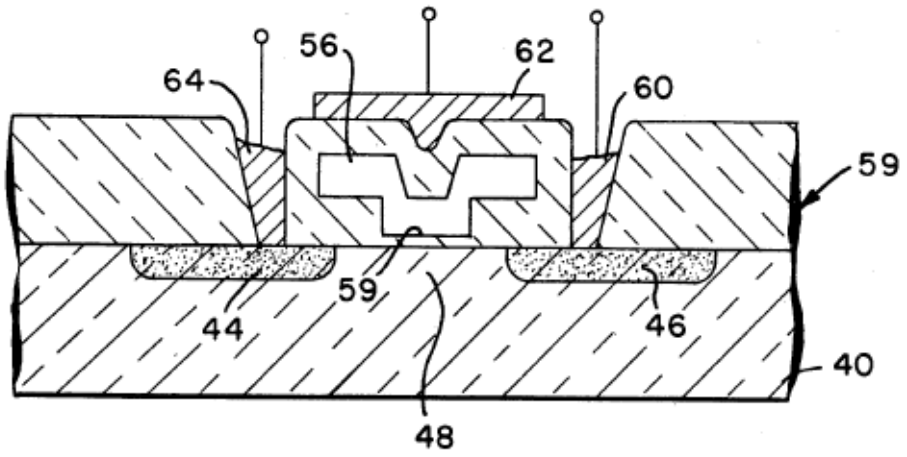
Primary Examiner—Gerald A. Dost
Attorney, Agent, or Firm—George Tacticos; W. H. MacAllister

[57] **ABSTRACT**

A non-volatile semiconductor storage device comprising a dual gate field effect transistor in which an electrically floating gate acts as a charge storage medium. An insulating layer of an appropriate dielectric material separates the floating gate from the active portion of the transistor. A predetermined section of this insulating layer is relatively thin to permit this section of the floating gate to be relatively close to a corresponding predetermined section of the transistor, thus facilitating the transfer of charges between the transistor substrate and the gate. When charges reach the floating gate either through tunneling or avalanche injection, they are entrapped and stored there, thus providing memory in the structure. That is, the electric field induced by these charges is maintained in the transistor even after the field inducing force is removed. Erasing is achieved by removing the charges from the floating gate by reverse tunneling through the relatively thinner insulator region.

12 Claims, 16 Drawing Figures



US005095344A

United States Patent [19]

Harari

[11] **Patent Number: 5,095,344**

[45] **Date of Patent: Mar. 10, 1992**

[54] HIGHLY COMPACT EPROM AND FLASH EEPROM DEVICES

[76] Inventor: **Eliyahou Harari**, 2320 Friars La., Los Altos, Calif. 94022

[21] Appl. No.: **204,175**

[22] Filed: **Jun. 8, 1988**

[51] **Int. Cl.**[5] **H01L 29/78**; H01L 27/01; H01L 29/10; H01L 29/40

[52] **U.S. Cl.** **357/23.5**; 357/23.1; 357/23.3; 357/41; 357/45; 357/53; 365/185

[58] **Field of Search** 357/23.5, 23.1, 23.3, 357/23.4, 41, 53, 45

[56] **References Cited**

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(List continued on next page.)

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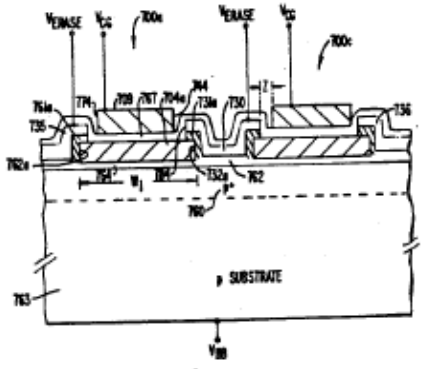
Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

Structures, methods of manufacturing and methods of use of electrically programmable read only memories (EPROM) and flash electrically erasable and programmable read only memories (EEPROM) include split channel and other cell configurations. An arrangement of elements and cooperative processes of manufacture provide self-alignment of the elements. An intelligent programming technique allows each memory cell to store more than the usual one bit of information. An intelligent erase algorithm prolongs the useful life of the memory cells. Use of these various features provides a memory having a very high storage density and a long life, making it particularly useful as a solid state memory in place of magnetic disk storage devices in computer systems.

15 Claims, 28 Drawing Sheets



Reference #5 (cover page)

US005172338A

United States Patent [19]

Mehrotra et al.

[11] **Patent Number: 5,172,338**

[45] **Date of Patent: Dec. 15, 1992**

[54] MULTI-STATE EEPROM READ AND WRITE CIRCUITS AND TECHNIQUES

[75] Inventors: **Sanjay Mehrotra**, Milpitas; **Eliyahou Harari**, Los Gatos; **Winston Lee**, San Francisco, all of Calif.

[73] Assignee: **Sundisk Corporation**, Santa Clara, Calif.

[21] Appl. No.: **508,273**

[22] Filed: **Apr. 11, 1990**

Related U.S. Application Data

[63] Continuation-in-part of Ser. No. 337,579, Apr. 13, 1989.

[51] **Int. Cl.**[5] **G11C 7/00**; G11C 29/00; G11C 16/04

[52] **U.S. Cl.** **365/185**; 365/201; 365/184; 365/195; 365/189.07

[58] **Field of Search** 365/168, 184, 185, 189.01, 365/189.07, 189.09, 201, 228, 104, 195; 371/21.4

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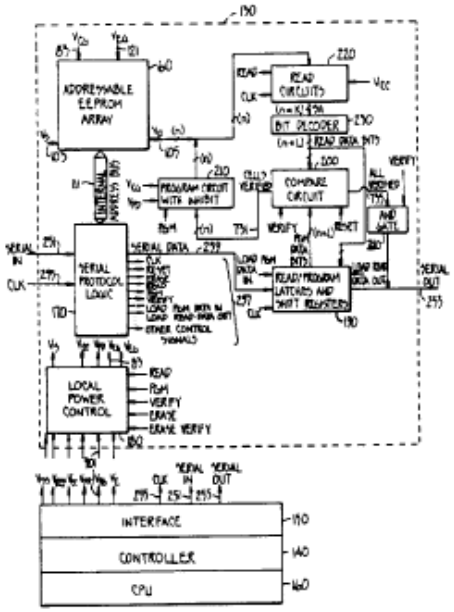
Primary Examiner—Alyssa H. Bowler
Attorney, Agent, or Firm—Majestic, Parsons, Siebert & Hsue

[57] **ABSTRACT**

Improvements in the circuits and techniques for read, write and erase of EEprom memory enable non-volatile multi-state memory to operate with enhanced performance over an extended period of time. In the improved circuits for normal read, and read between write or erase for verification, the reading is made relative to a set of threshold levels as provided by a corresponding set of reference cells which closely track and make adjustment for the variations presented by the memory cells. In one embodiment, each Flash sector of memory cells has its own reference cells for reading the cells in the sector, and a set of reference cells also exists for the whole memory chip acting as a master reference. In another embodiment, the reading is made relative to a set of threshold levels simultaneously by means of a one-to-many current mirror circuit. In improved write or erase circuits, verification of the written or erased data is done in parallel on a group of memory cells at a time and a circuit selectively inhibits further write or erase to those cells which have been correctly verified. Other improvements includes programming the ground state after erase, independent and variable power supply for the control gate of EEprom memory cells.

47 Claims, 21 Drawing Sheets



Reference #6 (cover page)

US005297148A

United States Patent [19]

Harari et al.

[11] **Patent Number: 5,297,148**

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[54] **FLASH EEPROM SYSTEM**

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[52] **U.S. Cl.** **371/10.2**; 371/10.1; 371/10.3; 365/200

[58] **Field of Search** 371/10.2, 10.1, 10.3, 371/40.1; 365/200

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[57] **ABSTRACT**

A system of Flash EEprom memory chips with controlling circuits serves as non-volatile memory such as that provided by magnetic disk drives. Improvements include selective multiple sector erase, in which any combinations of Flash sectors may be erased together. Selective sectors among the selected combination may also be de-selected during the erase operation. Another improvement is the ability to remap and replace defective cells with substitute cells. The remapping is performed automatically as soon as a defective cell is detected. When the number of defects in a Flash sector becomes large, the whole sector is remapped. Yet another improvement is the use of a write cache to reduce the number of writes to the Flash EEprom memory, thereby minimizing the stress to the device from undergoing too many write/erase cycling.

4 Claims, 5 Drawing Sheets