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Digitization Experiment of Television Standards Converter

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1. Foreword

A TV standard converter (TSC) using a delay line switching system has been developed (1) (2) (3) and put into practical use, but because it is an analog transmission system that uses a large number of ultrasonic delay lines, the configuration of the device is complicated and large, and requires advanced maintenance technology. In order to solve these problems, we have devised a method to digitize TV signals, use a large-capacity digital memory instead of an ultrasonic delay line as a memory element, and perform all conversion operations with digital signals.

2. Method and configuration of the experimental machine

In constructing the experimental machine, we focused on the following four items as elements for determining the method. (1) It must be an independent synchronous conversion system. (2) Both 625/50 → 525/60 and 525/60 → 625/50 conversion (including color 3 system and monochrome mode) must be possible. (3) Use general-purpose digital memory for the memory, which is the main part of the TSC, and minimize the amount of memory used. (4) It must have characteristics that surpass the delay line switching method. Of these items, (1) is achieved by making the memory input (WRITE) and output (READ) references completely independent synchronous signals. For item (3), the number of lines in the 525/60 format was used as the standard in order to minimize the number of lines to be stored in memory, and the VBL period and HBL period of each line that did not contain valid image information were not stored. In addition, the chroma signal is stored in a line-sequential manner to halve the storage capacity required for the chroma signal, and the bit structure of the general-purpose memory can be used as it is by code-combining with the luminance signal. For the memory, 16 stacks of 8KW, 18-bit computer wire memory were used for field interpolation. Table 1 outlines the decided schemes, and Fig. 1 shows a block diagram of conversion from the 625/50 scheme to the

525/60 scheme.

First, the conversion from 625/50 to 525/60 will be explained with reference to Fig. 1. The input is separated into luminance Y and color difference signals R-Y and B-Y by a 625/50 decoder. After sampling each signal at Y: 9 MHz, R-Y: 3 MHz, and B-Y: 3 MHz, the color difference signal (C) is multiplexed to 6 MHz. The multiplexed color difference signal C is coded with 6 bits, while Y is coded with 7 bits. After the encoded Y and C signals are interlaced and interpolated by line interpolation (ILI), the 9 MHz 7-bit Y signal and the line-sequential 3 MHz, 6-bit R-Y or B-Y signal are code-combined into 9 MHz 9-bit by the CODEPROC/circuit. In order to write this code-synthesized digital information to memory, a period longer than the memory cycle time (READ + WRITE = 1.2 μs) is required. In addition, a buffer memory (BUFF) is provided on the write side of the memory to perform memory readout priority control and eliminate the need for time correction on the output side. In the memory write operation, each field information is alternately written into two field memories A and B while performing line conversion. Memory readout operations are performed while performing field conversion (FC), while field interpolation (FI) is performed to correct discontinuous motion distortion caused by FC. Therefore, it is necessary to read out field memories A and B at the same time, so two readout terminals are provided. The output signal from these two output terminals is reversed from writing, namely parallel and series conversion (P-S CONV) and code decomposition (CODE PROC2). On the other hand, the chroma signal uses a 1-line digital delay line (1 HDL) to convert the line-sequential signal into a simultaneous signal (SE-SI CONV) to produce B-Y and R-Y signals, which are then passed through a D/A converter and LPF to become video output.

In 525/60 → 625/50 conversion, ILI control is performed after FI on the output side, and FC and line conversion are performed during memory readout.

3. Experimental result

The characteristics of the digital format conversion device are determined by the sampling frequency, encoding bit number, and interpolation method of the luminance and color difference signals.

Experimental results using the sampling frequency and bit number described above confirmed that DG and DP were within ±25° and ±2.5%, and S/N (Y) was 50 dB PEAK/rms or more. Figure 2 shows the vectorscope waveform of the NTSC output. In terms of stability, in particular, no unstable elements were observed during the experiment, and it is also characterized by the ability to obtain stable output images immediately after turning on the power.

4. Conclusion

With this experimental device, the objectives of high stability and miniaturization of the television standard format conversion device were achieved. For the time being, the interpolation method used is almost the same as the conventional delay line switching method, but in the future, we would like to proceed with comparative examination of various interpolation methods in order to further improve the performance.

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References

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Words in charts
Table 1
sampling frequency
number of bits
number of samples in one line
memory storage format
Memory storage code format
Required memory capacity

memory capacity
all
Delete 1 bit in 4 samples
Code combine Y and R-Y or B-Y to 9 MHz 9-bit (12 MHz 7-bit code combined to 9 MHz 9-bit)
244 lines
1 line = 492 x 9 bits
16 stacks, 1 stack = 8192 words 1 word = 18 bits
line sequence
( ) is for monochrome

Figure 1 625/50 → 525/60 conversion block diagram
1~256 lines
Internal SYNC

Figure 2 NTSC output waveform

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