Some Important Computers of Japanese Design

HIDETOSI TAKAHASI

Foreword

Hidetosi Takahasi's interesting chronology of the early work in Japan on computers was presented at the First USA–Japan Computer Conference, held in Tokyo in 1972 under the joint sponsorship of the American Federation of Information Processing Societies (AFIPS) and the Information Processing Society of Japan (IPSJ). That conference (as well as the following two) was organized with the intent of enhancing the mutual flow of information between Japan and the United States, acknowledging at the same time that developments in the United States were better known to the Japanese professional community than was the case in the other direction.[1]

To help establish some background for the paper, it may be helpful to outline how the events described fit into the chronology of computer development in Japan. To do this, it is convenient to consider events in the Japanese computer industry as separated into three consecutive time phases. (Some readers may not agree with my arbitrary definitions for the transitions or the groupings, but the basic sequence is valid.)

The first phase, which is in fact the time period covered in Takahasi's[2] paper, encompasses a relatively unstructured time, when individuals, universities, and companies were participating in separate and sporadic development activities.

The second phase, described by Takahasi in terms of "second-generation machines, from the late 1960s," is characterized by six to ten major licensing agreements by Japanese companies with United States and (to a limited extent) European computer companies.

The third phase, which was evolving at the time Takahasi's paper was published, began as a progressive loosening of these formal technological licensing agreements, followed by temporary pairings of the major Japanese computer manufacturers under government encouragement (translation: contracts) on specific development projects. This third phase marked the entry of several of the Japanese companies into the world marketplace as independent and technologically advanced computer manufacturers.

For those interested in the evolution of the Japanese computer industry, the first and third phases have, for different reasons, more significance than the second. The second phase was a transitional one, when most of the major computers made in Japan were built under license for domestic use, and therefore were similar in performance and characteristics to machines available abroad.

The three phases of the Japanese computer industry have been influenced not only by computer technology but also, in the latter stages, by policies supported by the Japanese government. There are counterpart examples in other industries. Following the end of World War II, the government set out to rebuild the country by defining policies aimed at reconstructing the economic sector. During that period, national policy encouraged the development of heavy industries such as steel, automobiles, chemicals, textiles, and shipbuilding.

Having established a competent and competitive capability in heavy industry, ministries in the government defined a national information policy, with the goal of developing a "knowledge industry."

Takahasi's paper goes back to a quieter and more uncertain era, when computers, not only in Japan but everywhere, were considered technologically and intellectually important, but not yet having their current commercial and financial influence.

The comments in Takahasi's paper make very clear how limited were the resources available to the pioneers in Japan, in striking parallel to the situation in Europe and in those United States organizations not directly involved in specific government-funded programs. Although many of the events and issues discussed in the article coincide with the evolution of system concepts and components everywhere, the activities in Japan during that time are not well known in the West. The paper provides an interesting corroboration of the similarity of worldwide events at that time, when resources were limited, computer commerce was still unstructured, and development was not yet focused by financial and political forces.

Discussing the period from the late 1940s to 1965, Takahasi describes Japanese computers using relays, vacuum tubes, parametrons, and, finally, transistors. There is historical interest in all four of these topics, but the topic that least parallels developments elsewhere is the parametron. The original invention of the parametron was by Eiichi Goto at Tokyo University. The parametron, based on magnetic phenomena, was publicized throughout the world, and Goto was widely recognized for that achievement.

Progress in solid-state technology and the advantages of semiconductors made magnetic techniques, other than for memories, obsolete. (But even technology recycles; some of the current work on switched power supplies is using magnetic logic.) It is interesting to speculate about what might have happened had semiconductors not developed as quickly as they did, or if thin-film developments in magnetics had made the parametron faster or more economical.

The Takahasi paper—and others describing the history of computer activities in Japan from the inside—is recommended to all who seek to understand the foundations of an established and growing segment of the industry.

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[1] Richard Tanaka was responsible for initiating all three of the USA–Japan Computer Conferences and served as the honorary cochairman for them from the United States.

[2] The reader may notice, not only in Takahasi's article but also in others from Japan, an apparent discrepancy in the spelling of the syllable pronounced "shē" and spelled both "si" and "shi." The latter is the currently common phonetic spelling; the former represents a convention established earlier but modified in the late 1940s or early 1950s. In following the *Annals* style of not using titles, the honorific "Professor" has been omitted from Takahasi's name; it would certainly be used in Japan.

1. Introduction

Rapid growth of the computer industry is one of the most striking events in the "miraculous" industrial explosion of postwar Japan. At the time the ENIAC was completed at the Moore School of Electrical Engineering, we were on the verge of starvation in the ruin of our defeated country. When we learned of the astonishing power of the "giant brain," it seemed indeed to be something belonging to another world. We were starved for knowledge as well as for food, and some of us who were optimistic enough were inspired by this fascinating new technology. We decided to make our own computers, and the study of "mechanical brains" got under way in Japan.

Strictly speaking, the idea of doing digital calculation with electricity was not unknown in Japan at that time. Fuji Electric Works (of which Fujitsu was an affiliate) had built a small four-arithmetic calculator using relays in 1941. Hideo Yamashita of the University of Tokyo had the idea of constructing a sorting and totalizing machine (Yamashita 1951) using relays to replace the card-consuming punched-card machines for statistical surveying. The actual machine was completed in 1948. It is interesting to note that both of these relay machines used binary representation of numbers.

Also important is the work of Nakajima and Hanzawa (1936; 1937) on the use of Boolean algebra to build relay contact networks. Their work was inherited by a number of communication engineers. The existence of this background accounts for the rapid progress in digital technology in Japan during and after the 1950s.

Around 1950, however, it was difficult to foresee the importance of digital technology as it is today. Few people in electronic manufacturing seemed to show any interest in digital computers, which would cost them billions of yen to develop, with one exception: Fujitsu.

In such a situation, it was natural that the first project on a large-scale machine concern the relay computer, because we already had a good deal of experience in the design, construction, and maintenance of a large system composed of tens of thousands of relays. In the Electrotechnical Laboratory (ETL), a project was launched by Mochinori Goto to build an automatic calculator as an application of his theory on relay networks. ETL designed a small-scale pilot machine, the ETL Mark I, and completed it in December 1952. A full-scale machine, the ETL Mark II (Goto et al. 1955), was subsequently designed; it began operation in November 1955. Fujitsu, which cooperated with ETL in the construction of these machines, also designed its own machines, and FACOM 100, the first full-scale machine, began operation in October 1954. Fujitsu also designed much more elaborate models, the FACOM 128A and 128B (Ikeda et al. 1958).

Some of those inspired by the news of ENIAC went on to basic research in electronic computers. Among them were Kenzo Joh of Osaka University and Bunzi Okazaki of Fuji Film Co. In March 1956 Okazaki finally ran a problem on his machine, the Fujic (Yamashita 1960), which is honored as the first electronic computer built in Japan. The TAC project ("Report on the Todai Automatic Computer" 1962)

was organized jointly by the University of Tokyo and Tokyo Shibaura Electric Co. The path was not smooth for this project, but TAC was at last ready in January 1959. These two machines were the only ones that used electron tubes.

The huge expense and lack of experience in the operation of extremely complex systems made people hesitate even though they had much interest in building a computer. It was evident that electron-tube machines would cause too much trouble to operate and maintain, even if we could afford to build one. We had to find some logic element that was more stable and less expensive. Magnetic core logic seemed to be one promising candidate.

In March 1954, the very thing we had awaited appeared: the parametron (Takahasi and Kiyasu 1960). A joint research team was organized by the University of Tokyo, Nippon Telephone & Telegraph (NTT), and Kokusai Denshin Denwa Co. (KDD) to start intensive work for the development of the parametron as a computer element. One year later, when the technical know-how of this research was partially released, quite a number of manufacturers began to study the parametron for the purpose of building their own computers.

The M-1 (Muroga and Takashima 1959) of the Electrical Communication Laboratory of NTT was the first computer to get into preliminary use with a very small memory. The HIPAC-1 of Hitachi, the PC-1 of the University of Tokyo (Takahasi 1968), the NEAC 1101 of Nippon Electric, and others followed. Several commercial machines came thereafter, including some very simple ones that replaced punched-card machines.

The Electrotechnical Laboratory, on the other hand, recognized the importance of the transistor as a computer component, and decided to concentrate on its development. The first machine, the ETL Mark III, was completed in July 1956. Its reliability was unsatisfactory because of frequent failure of transistors, which were now obsolete point-contact transistors. ETL soon went on to build another computer using junction-type transistors, the Mark IV (Nishino et al. 1959). The Mark IV worked quite satisfactorily, and it became the prototype of several commercial transistor computers, such as the HITAC 301 of Hitachi and the NEAC 2201 and 2203 of Nippon Electric.

In the following I will describe some of the early Japanese machines that are thought to be of special historical or technical interest. Second-generation machines, from the late 1960s, were mostly the product of technical cooperation with American manufacturers and were therefore more or less patterned after their partners' designs, if not a direct copy. I will describe just one machine, the HITAC 5020 of Hitachi (Nakazawa et al. 1964), as one of the very few exceptions to this statement.

2. Relay Computers

The ETL Mark II was the second full-scale relay computer built in Japan, designed by the Mathematics Research Group of the Electrotechnical Laboratory of the Ministry of International Trade and Industry. The project was organized by Mochinori Goto, and the chief designer was Yasuo Komamiya. The machine was completed in November 1955.

The Mark II, as well as its pilot model, the Mark I, was said to be the result of application of a general theory of relay networks by Goto and Komamiya. Unlike the Harvard machines, the ETL machines employed completely asynchronous circuitry. One reason for this decision was that a relay with exposed metallic contacts is a component with less reliability and stability than electron tubes and transistors, if it is used in a similar manner. Its time lag is subject to much greater variation; consequently, if it is used in a synchronous circuit as in most electronic computers, the clock rate must be kept rather low to allow for the variation of the operating times. Since speed was the main goal in the design of these machines, use of asynchronous logic was a natural outcome, especially if one considers that it is the more established technology.

To attain the utmost in speed and reliability, the following general rules were laid out as guiding principles:

1. The main chain of events within the circuit propagates only as contacts are made, since this gives least operational delay.
2. Every relay A_k is accompanied by a conjugate relay $\bar{A}_k$, such that after completion of operation, either A_k or $\bar{A}_k$ is energized. Rule 1 can be satisfied on account of the use of this paired logic.
3. The whole operational unit is released at once after completion of operation is checked by testing whether rule 2 is actually satisfied.

A retrying scheme was also used so that when the machine remained halted for a certain duration, the unit operation was started again with the same initial state. Thanks to the adoption of the above rules and the retry feature, practically every possibility of undetected error was eliminated. The only exception to rule 2 was the main memory, which used only one relay to store one bit. This was actually the weakest point of the system.

The ETL Mark II was a binary floating-point machine. Conversion of decimal input data to binary form was done by a special unit in the tape-preparation stage, so that the input tape was binary with one hole for each zero or one. Binary-to-decimal conversion was also done during output by special hardware. The main reason for adopting the binary system was to economize on the main memory, which was an extremely expensive and bulky part of the machine.

The machine was built of specially designed relays of several different types. A paper-tape reader and tape perforator were also specially designed for use with 6-hole tapes.

Each instruction in the ETL Mark II caused transfer of numerical data via a bus by specifying the addresses of the in gate and the out gate. Most of these gates were for the main memory, but some were for registers associated with some arithmetic operations, so that operation could be specified. An address-modification facility was also provided.

The FACOM 128A/B was a commercial relay computer manufactured by the Fuji Tsushinki Seizo K.K. (Fujitsu Ltd.), which had cooperated with ETL in constructing the ETL Mark II. It was designed on the basis of experience with an experimental computer, FACOM 100, completed in October 1954 as the first full-scale automatic computer in Japan. The first system of FACOM 128A was delivered in May 1956 and installed in the FACOM Computing Center of the Yurin Electric Co.

Like the ETL machines, it had asynchronous logic, but it was decimal and used standard three-address instructions. Its logic design philosophy was fundamentally the same as in the ETL machines, but a little more sophisticated. Each decimal digit was represented in biquinary form internally. Its checking system, instead of checking each unit operation separately before going ahead, proceeded at full speed with the main chain. The checking operation formed another chain process that propagated after the main computation. A speed of 0.1–0.35 ms for floating-point multiplication was thus obtained.

In addition to its main memory of 185 words made of cross-bar switches, FACOM 128B had 80 words of constant (wired) memory. There were also 200 words of read-only memory for programs using punched cards. Library routines of about 500 instructions were permanently wired to the machine, including such routines as double-precision arithmetic, matrix inversion, and standard functions.

FACOM 128B was characterized by a versatile set of instructions. In addition to the indexing facilities for address modification and cycle counting, it had special instructions for subroutine call with automatic return, polynomial evaluation, masking operation, etc. Instructions were also provided to facilitate multiple-precision calculation. Indexing calculations were done in parallel with the main calculation so they usually did not require extra time. All these special facilities served to increase the overall speed of the machine. In a certain sense, FACOM 128B can be said to have attained the practical limit of the speed of a relay computer.

Two FACOM 128As and six 128Bs were manufactured. The 128B installed in Nippon University in Tokyo is now [1980] at Ikeda Memorial Museum in Fujitsu's Numazu plant, where it is still in operating condition.

3. Vacuum-Tube Computers

The Fujic, a vacuum-tube computer built by Bunzi Okazaki of the Fuji Film Co., was the first electronic computer built in Japan, and consequently the first stored-program computer in Japan. At the time of its completion—March 1956—the only "electronic" computer imported was the UNIVAC 60/120 calculating punch.

Okazaki conceived of the construction of Fujic with the hope of speeding the design of photographic lenses. He used 8-channel mercury delay lines for memory, with a capacity of 256 words of serial 34 bits. The clock rate for memory was 1 MHz, but the main logic operated at 30 KHz in parallel mode. It was a binary, three-address, fixed-point machine, designed with special emphasis on ease of programming. For numerical words, the binary point was placed to the right of the four leftmost bits, so most of the important numerical constants could be represented without scaling. The input instruction read

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a row of holes from a card and placed it directly in the memory with necessary conversions. The output instruction printed the contents of a word in the memory by an electric typewriter after conversion to decimal form, where the number of digits, label, sign, decimal point, and all other format specifications were given in the address part of the instruction. This hardware-oriented input/output scheme requiring no input and output routines was chosen as the best alternative in an environment where few professional programmers were available.

The main part of this historic machine is now [1980] exhibited in the Science Museum at Ueno Park in Tokyo.

The TAC was a vacuum-tube computer with Williams tube memory designed and built by a joint effort of the University of Tokyo and the Tokyo Shibaura Electric Co. (Toshiba). The project started in early 1952, but progress was hampered by the appearance of countless unexpected troubles, so it was not ready until 1959.

External specifications of the TAC were almost identical to those of EDSAC I in Cambridge, but with the important addition of a full set of floating-point arithmetic instructions. This feature seemed rather ambitious at the time of the start of the plan. After completion, the TAC was used for scientific work for two years and then dismantled. The Williams tube memory remained the most vulnerable component all through the life of the TAC, but one interesting story of its memory is that its storage capacity was doubled overnight, from 256 to 512 words, by a fine readjustment of the focusing system.

4. Parametron Computers

As mentioned in the introduction, a number of computers were built using parametrons during the early times. The parametron was a computer component consisting of nonlinear coils, a capacitor, and a resistor, and was driven by a specially modulated high-frequency power supply. Since it was extremely simple in structure and contained no semiconductor component, the parametron was characterized by extreme ruggedness, reliability, and long life. It was also very inexpensive compared to transistor logic at the time it was being developed (about 200 yen per unit when mass produced). Its further advantage was that it was a universal element in the sense that it performed all functions required for a logic element—namely, amplification (fan-out), delay, and logical operation. In principle, the whole computer could be built of parametrons only.

The parametron was invented by Eiichi Goto in March 1954, and several digital devices with thousands of parametrons were built in and around 1956, but construction of stored-program digital computers with parametrons had to wait until a satisfactory memory device became available that could be used with a parametron network.

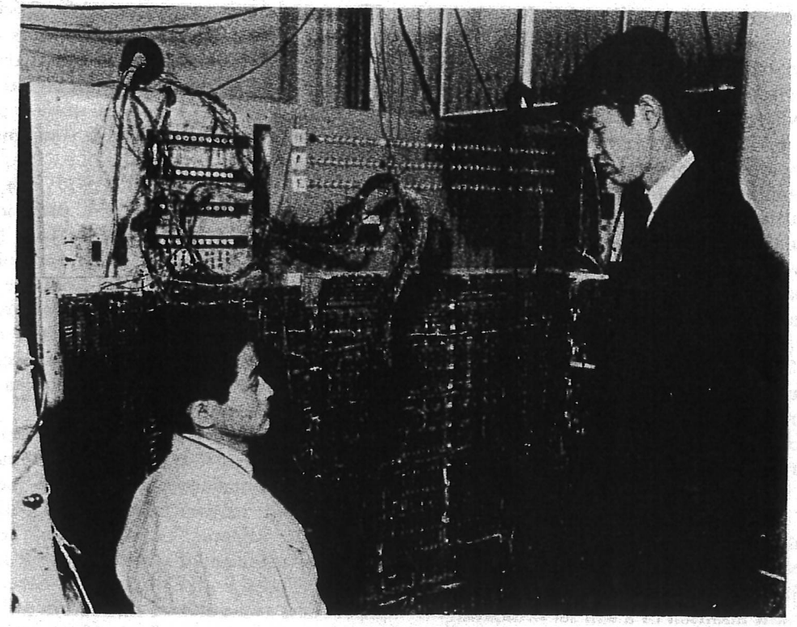
The first working model of a parametron computer, the M-1, was completed in April 1957 at the Electrical Communication Laboratory of NTT. Its name, Musasino-1, was derived from the city where the laboratory is located. The architecture of the M-1 was almost identical to the ILLIAC I of the University of Illinois and was chosen because NTT wanted to use the famous library routines of ILLIAC without modification.

The M-1, as well as many other parametron computers, used "dual-frequency" core memory. It was essentially a word-arrangement core memory, but differed from conventional ones in the writing and reading scheme. To write into the core, one applied two sinusoidal currents having a frequency ratio of 1:2 on the wire through the core. Superposition of these two currents resulted in a magnetizing field of asymmetric waveform, which magnetized the core in a definite direction. To read out, one applied a sinusoidal current and detected the second harmonic component of the induced voltage. This scheme had an advantage for use with parametron logic: the input and output signals had the same form as that of the parametron. With a conventional system, one had to use converters between the phase-modulated signal and the pulse signal, using diodes and transistors, which were less reliable components.

At the time the logic part of the M-1 was finished, development of this core memory was still underway, and the M-1 had to be used with a pilot-model memory of only 32 words for one year. This one-year test run gave profitable data on continuous operation of a large parametron device. It proved that the outstanding characteristics of the parametron were stability and reliability.

The M-1 was equipped with a full core memory of 256 words in April 1958. A computer with the same basic design but with expanded memory capacity was made commercially available from Fujitsu with the name FACOM 201.

The PC-1 was an experimental parametron computer built in our own laboratory in the Physics Department of the University of Tokyo. It began to work as a stored-program computer in March 1958,



The parametron computer PC-1, in the spring of 1958 when it was operating but not yet completed. Eiichi Goto is on the left; Hidetosi Takahasi on the right.

without multiply and divide instructions. Installation of these missing instructions was completed in August 1958, but many programs were run without them.

The PC-1 had a dual-frequency core memory of 256 words of 36 bits. Its memory-driving circuit used a word selector incorporating the error-correcting code and the load-sharing matrix. It had 18 sinusoidal wave generators, which fed the pumping coils of $2^8 = 256$ parametron subharmonic generators via a transformer matrix. Owing to the threshold property of parametric oscillation, only one of the 256 parametrons could oscillate, and this parametron supplied the read/write current for the selected word. This scheme had a unique feature: one or two tubes could fail without causing any malfunction of the memory.

The arithmetic unit was built around a universal adder having a high-speed carry logic. In this adder, all the carry digits were generated in parallel by separate logic networks so that logical delay for carry generation was proportional only to the logarithm of the number of bits in a word. Thanks to this adder and the core memory, PC-1 was the fastest computer in Japan for a year or two, in spite of the low clock rate (about 10 KHz). Another artifice to increase the speed was the overlapping control scheme.

The PC-1 was a single-address, fixed-point machine. Its numerical word had a long/short option as in EDSAC I. Its architecture was fairly conventional except for a few special features mentioned below. Input and output instructions had a busy-jump feature, which was unique at the time. In conjunction with the interrupt facility, which was added in summer 1959, it enabled output buffering by software to eliminate the loss due to waiting time. This might be called a primitive form of multiprogramming.

The PC-2 was a larger parametron computer designed by our team in collaboration with Fujitsu. It was completed in August 1961. Its design philosophy was essentially the same as the PC-1, but it incorporated many more facilities and used more sophisticated logic design. Electronically, it was the first and only parametron machine to use a pumping frequency of 6 MHz. The modulation (clock) frequency was correspondingly increased to about 66 KHz. Use of this high pumping frequency together with the increased size (13,000 parametrons) necessitated special precautions to equalize the phase shift along the feeder line and the internal wiring. Even with such precautions, we had to grapple with countless unanticipated troubles during circuit adjustment.

The logic design followed in general the same principles as the PC-1, but was more sophisticated. In order to increase the speed, multiplication was done in modified quaternary form. In each stage of division, it prepared two temporary residues for the cases of quotient bit being zero or one, and the correct one was selected as soon as the quotient bit was determined.

The control of the PC-2 had an overlapping feature that allowed two instruction flows to run in parallel. Thus, when one or more "housekeeping" instructions (ones not using the accumulator) followed an arithmetic instruction, the former were allowed to run concurrently with the arithmetic instruction, so the one long arithmetic instruction (multiplication or division) could absorb the operation time of several housekeeping instructions that followed it, if instructions of both types were distributed in an appropriate manner.

The table search instruction, with a variety of searching conditions, was one of the PC-2's most powerful instructions. A square-root instruction was included because of its importance in scientific calculations. Provision of double-precision floating-point instructions was also a rather ambitious concept at that time. An indirect addressing feature was not provided, but its "execute" instruction could be used in its place in most cases.

The PC-2 could handle eight magnetic tape units. While the "channel" concept was not adopted, its tape control system was powerful enough with its unique design. A presettable counter was provided for each tape unit to count the block marks on the tape until it overflowed and caused interruption. This enabled block search to be run off line, so that concurrent operation of several tape units could be done with no difficulty.

The HIPAC (Hitachi Parametron Computer) 101 (Takeda et al. 1960) was the first commercial parametron computer manufactured by Hitachi Electric Works. Its design was based on the experimental computer HIPAC 1, which was completed in August 1958 and was therefore the first parametron computer to go into full operation. The machine used a magnetic drum for the main memory. This may be said to be a thoughtful decision because the development of core memory was still full of unknown factors at the time these machines were designed.

The HIPAC 101 was a binary, single-address, fixed-point machine, with a memory capacity of 2048 words. It had two index registers and a relative addressing facility. It was exhibited together with Nippon Electric's NEAC 2201 at the International Computer Exhibition in Paris in 1959, held in conjunction wth the UNESCO Information Processing Conference. Hitachi engineers were proud of the fact that after shipment by air from the other side of the earth, the machine was unpacked, installed, and working well without any readjustment—a dramatic demonstration of the stability and ruggedness of the parametron.

Unlike the PC-1 and M-1, the HIPAC's parametron units were mounted on a plug-in package, which enabled use of the ordinary wiring procedure of soldering or wrapping wires on pins. This might be preferable to the rather unconventional procedure of bringing wires through toroidal cores, when the machine is to be assembled in an ordinary production line.

The HIPAC 103 was a medium-size parametron computer for scientific use. The first one was delivered in August 1961 to the Kansai Electric Power Co. Its main memory consisted of ordinary core memory of 1024-4096 words and a magnetic drum, the total capacity being 8192. Since the capacity of the drum was also 8192, the remaining part of the drum could be accessed by block exchange between the core and the drum. Several systems of the HIPAC 103 are still [1972] in use.

The SENAC (Katsura 1959) or NEAC 1102 was designed and constructed jointly by Tohoku University and Nippon Electric Co. It was a rather large parametron computer using 9600 parametrons and a 1024-word magnetic drum memory. Its numerical words consisted of a 40-bit mantissa and an 8-bit exponent. For fixed-point calculation, only the mantissa part was used. Five index registers were provided. The machine had a versatile instruction set including immediate operand instructions, instructions facilitating double-length calculations, etc. Floating-point and fixed-point operations were represented by the same instruction; one was selected by a flip-flop set and reset by a switch instruction.

5. Transistor Computers

The ETL Mark IV was a decimal computer using 470 transistors and a magnetic drum memory of 1000 words. It went to work in November 1957 and may be said to be the first transistor computer in Japan that was successfully operated for actual work. Its logic package was mainly composed of a dynamic flip-flop with and-or gates. Clock frequency was 180 KHz. Numbers were represented in serioparallel

mode, and average multiplication time was 4.8 ms inclusive of access time. The basic know-how of the ETL Mark IV was used in constructing the HITAC 301 of Hitachi and the NEAC 2201 and 2203 of Nippon Electric.

Of the low-priced transistor machines, OKITAC 5090 (Fujii 1962), built by Oki Electric Co., was the first one equipped with a core memory. Although essentially a decimal machine, it provided binary instructions so that bit handling could be done efficiently. A floating-point option was also available. The maximum memory capacity was 4000 words of 49 bits (12 decimal places plus sign). The outstanding feature was the output line printer, which was included in the standard configuration. A choice of system configuration ranging from A to D was available, so OKITAC 5090 could be adapted to both scientific and business applications.

The Hitachi HITAC 5020—in operation in the spring of 1965 at Kyoto University—can be called the first large-scale computer built in Japan. The HITAC 5020 was supplied with up to 64K words in core memory and a wide choice of peripheral equipment. Memory protection and other facilities were provided to allow monitored operation.

In order to get a high speed with a small amount of hardware, serial logic was adopted with a clock rate of 18 MHz. Electromagnetic delay lines were used as accumulators and other special registers. Of the fifteen accumulators, seven also served as index registers. Multiplication time was 36 microseconds in floating point.

The standard word length was 32 bits. Instructions were of either single-word or double-word type. Double-word instructions were mostly of variable word length with bit addressing that provided a large variety of bit-handling operations. There were also repeat-type instructions that effectively executed simple loop programs in a single instruction. These various types of instructions were very powerful in bit-pattern handling.

The HITAC 5020E was an expanded model that was about six times as fast as the 5020. This increase in speed was obtained by use of partially parallel addition in multiplication, adoption of advance control, etc. Several additional instructions were included in the 5020E, such as quadruple-precision floating-point arithmetic operations, which were done in the 5020 by "software instructions."

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