INCORPORATING AC VOLTAGE REGULATION IN HVDC SCHEME CONTROLLERS AND DESIGNS

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ABSTRACT

A new economic and effective scheme for controlling the ac voltage at the HVDC terminals during both steady state and dynamic conditions is presented. By extending the basic characteristics of an HVDC converter, it is possible to affect and modulate the reactive power balance on the ac side. To incorporate such a feature in an HVDC scheme, certain additions and modifications are required to be made in the operation and control of HVDC converters. Analytical studies as well as digital and simulator results are presented to demonstrate the viability of the proposed ac voltage control strategy to optimize HVDC terminal design and performance for a practical example. The economic and technical features of the new scheme are discussed in comparison to other ac voltage control techniques such as synchronous condensers and static VAr compensators.

INTRODUCTION

HVDC converters of dc transmission or back-to-back schemes require reactive power at their commutating ac bus for their operation. Due to the delay angles associated with commutation overlap and dc current or dc voltage controllers and to avoid commutation failures, the ac fundamental current at an HVDC terminal always lags the ac commutating voltage. Whether in rectifier or inverter mode of operation, dc converter terminals absorb reactive power in proportion to their real power conversion. For conventional HVDC schemes, this proportion is approximately 60% during steady state conditions. If the host ac system has a relatively high source impedance, it cannot supply this reactive power without the ac bus voltage falling to an unacceptable low level. To avoid this, compensating shunt capacitor banks are oftentimes applied at the ac bus of the HVDC terminal. Some of these banks also serve as harmonic filters to short circuit the harmonic currents generated by the converters. However, the reactive power absorption by the dc converter is not always constant and can widely vary especially following major disturbances. Therefore, a sudden disturbance in the reactive power balance would cause, in this case, high power frequency overvoltages[1]. These overvoltages are usually an essential factor in the design of most of the HVDC converter compo-

nents and its associated ac apparatus. To include such high overvoltages in the design of the dc converter terminal is quite costly besides the fact that they will be transmitted to other parts of the network along the ac transmission and distribution systems. In this case, all apparatus will be subjected to high voltage stresses which can often exceed their design value. A prime objective would then be to limit such overvoltages in an economic and effective manner. Fast corrective measures are, therefore, always called upon to regulate the net reactive power exchanged with the ac system at the dc converter terminal and maintain its ac voltage within permissible limits[23] The HVDC converter design can then be optimized in terms of cost and overall system performance. For this purpose, synchronous condensers and static VAr compensators have been considered. However, they constitute an additional equipment that has to be added to the total cost of the HVDC converter terminal.

A new economic ac voltage control technique is developed to effectively control the ac voltage during steady state conditions and to limit its excursions following ac or dc system disturbances. By only extending the basic characteristics of an HVDC converter, it is possible to affect and modulate the reactive power balance at the interconnecting ac bus[46].To achieve such a feature in a HVDC scheme, certain additions and modifications are required in the operation and design of HVDC converters. By this method, the HVDC terminals can be made self sufficient in terms of ac voltage control, thus making an HVDC scheme more economically attractive. This new principle of operation and control is the subject of this paper.

Problems of ac voltage regulation and instability at an HVDC terminal are first quantified analytically by means of a simplified mathematical model. To prove the viability of the proposed control strategy, digital as well as HVDC simulator simulations are presented for the complete ac/dc systems of practical cases. The economic and technical features of the new scheme are also demonstrated in comparison to synchronous condensers and static VAr compensators.

PROBLEMS OF AC VOLTAGE STABILITY AT AN HVDC CONVERTER

Large ac voltage fluctuations are considered to be a persistent problem associated with HVDC schemes when connected to relatively weak ac systems. To estimate the extent of those voltage variations, the criterion of short circuit ratio (SCR = short circuit capacity of the ac system at the HVDC converter site/nominal dc power) has consistently been used. However, such a simplistic approach does not take into consideration the voltage/reactive power characteristics of the ac network nor the operating control mode of the HVDC scheme. It is also not suitable for including the effects of static means for voltage support. Therefore, it is essential to define a more adequate criterion for ac voltage sensitivity in which the effects of HVDC operating and control modes, ac system damping as well as reactive power compensation methods can be taken into account.

In this section, a new approach is presented to quantitatively determine the regions for potential voltage instability at the ac/dc junction.

In order to establish the voltage stability criterion and to fully examine the influence of various system parameters and operating conditions, an appropriate simplified mathematical model is developed. The model representing the ac/dc interconnection point is as shown in Fig. 1. In this model the ac system is represented by constant voltage sources behind fixed impedances, i.e. constant impedance loads. The total reactive power demand of all ac lines terminated at the interconnection point to maintain a constant voltage V at the HVDC terminal is Qac. For the case studied, where the short circuit ratio SCR at the dc rectifier terminal is 2.4, the variation of Qac as a function of dc power transmitted is as shown in Fig. 2. Both Qac and Pdc are expressed in per-unit basd on nominal dc power Pdn.

The HVDC converter is modeled by its linearized system of equations where small variations of dc current, dc voltage and firing (or extinction) angle are allowed. Fixed converter transformer taps are assumed. Reactive power compensation at the HVDC terminal is first assumed to be carried out by means of filters and capacitor banks. These can be represented in the fundamental system frequency as a lumped shunt capacitive sucseptance Bc.

As a measure of ac voltage stability, the "Voltage Stability Factor" VSF is defined at a specific dc power level Pd as:

$$VSF = \Delta V / \Delta Bc$$

where ΔV is the incremental voltage change due to a small change in the shunt capacitance ΔBc.

The voltage stability factor "VSF" can be determined as a function of dc power transmitted as shown in Fig. 3 for different operating conditions. If the system is assumed to have a SCR = 3.5 and the dc converter is operating in a conventional mode of operation, say with constant firing (or extinction) angle, VSF will be as shown by curve (a) in Fig. 3. As expected for this strong ac system condition, small variations of ΔV are experienced at low dc power levels whereas relatively higher variations - but with limited magnitude - take place at higher Pdc as a result of changing the capacitance ΔBc. However, when the ac system is weaker, say with SCR of 2.4, but with the same Qac/Pdc characteristics the VSF is depicted as shown in Fig. 3 (curve b). Under such conditions a region of potential ac voltage instability occurs in the vicinity of 0.8 pu dc power level where large excursions of ac voltage can arise on account of any small variation in the shunt capacitance Bc. When the dc converter is operating with constant dc current, similar ac voltage instability characteristics are produced.
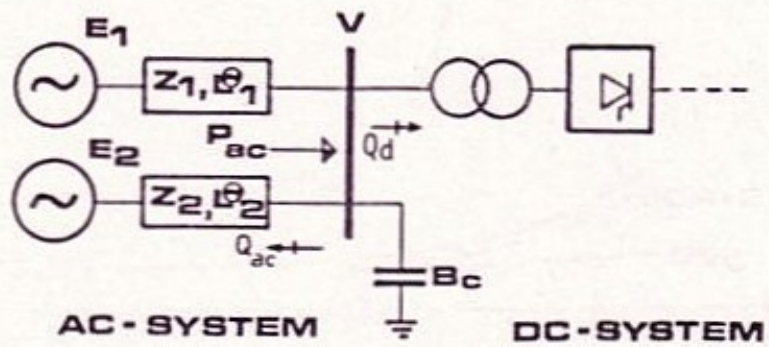
Fig. 1.   Simplified system model for ac/dc interconnection point
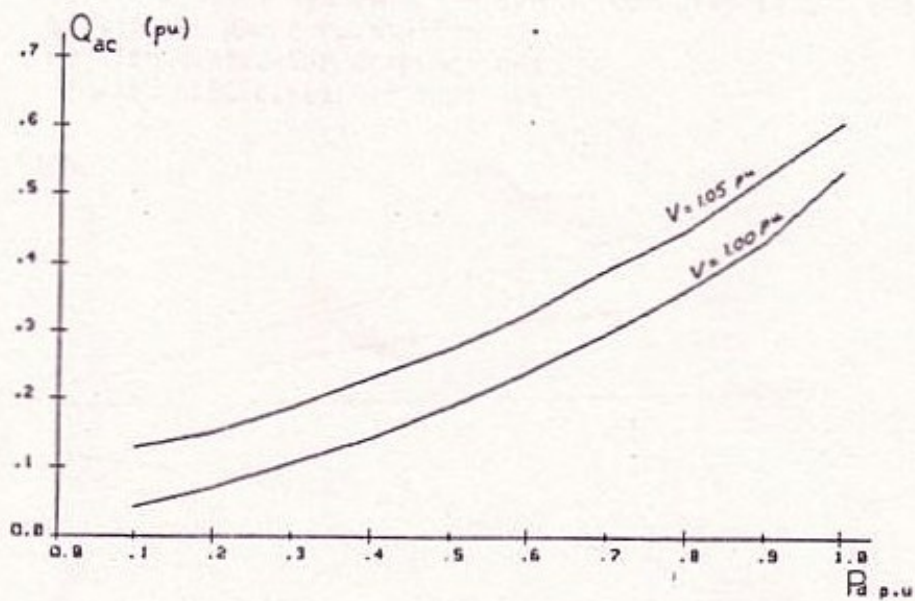

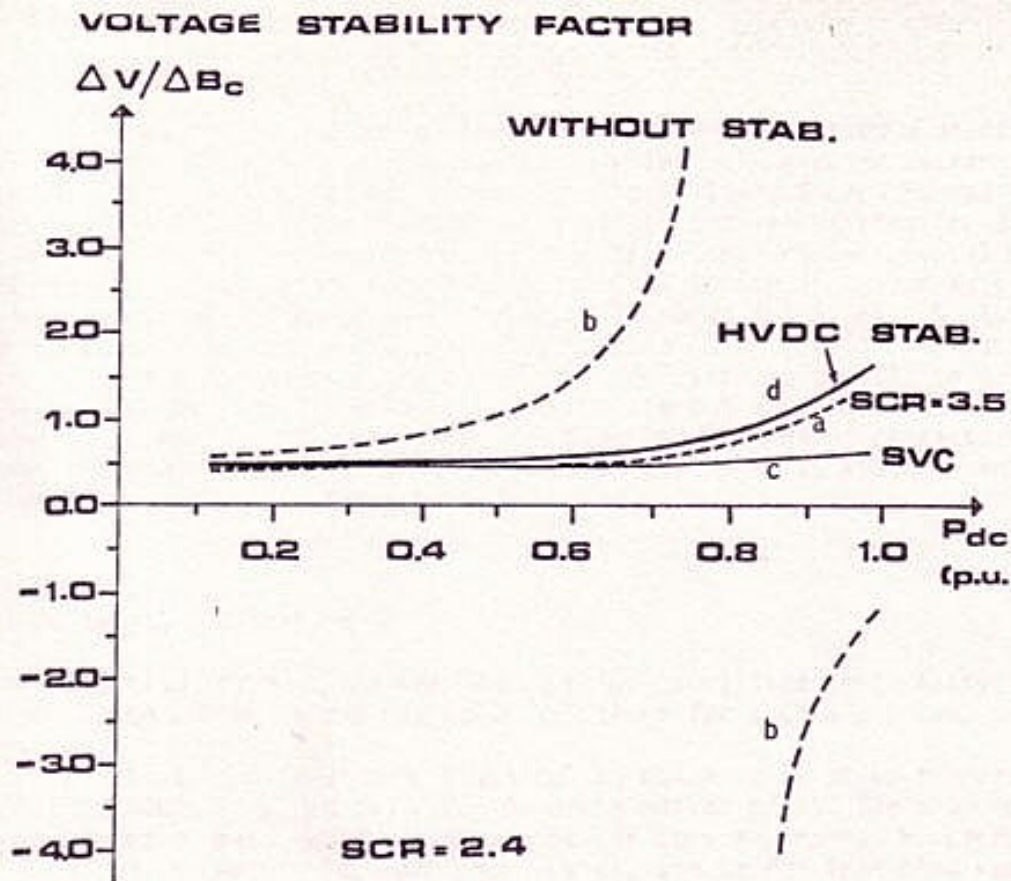Fig. 2.   Total reactive power demand of ac network at HVDC converter terminal

Fig. 3. Voltage Stability Factor for different VAr compensating schemes (SCR = 2.4):
a) for a stiff system (with synch. condensers) SCR = 3.5
b) with no VAr compensation
c) with static VAr compensators
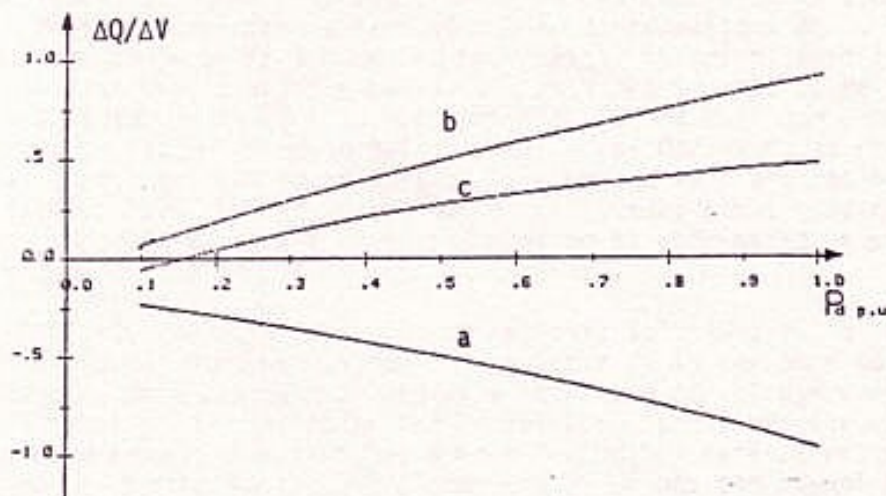d) with HVDC converter controls

Fig. 4. Linearized ac/dc system performance ($\Delta Qd/\Delta V$) for:
a) system with no VAr compensation
b) system with static VAr compensator ($\Delta Qd + \Delta Qs$)/ΔV
c) system with HVDC converter controls

Two major reasons can be thought of to be behind such a phenomenon: a) that complete VAr compensation for a relatively weak ac system is attempted by means of static shunt elements (filters & capacitors) and b) that the HVDC converter operates with almost the same firing (or extinction) angle near its minimum value. In this case the incremental change of reactive power absorbed by the dc terminal to the change of ac voltage ($\Delta Qd/\Delta V$) is always negative as depicted by curve (a) in Fig. 4. This example clearly shows that inspite that SCR can still give an indication of the overall properties of the combined ac/dc system, it fails to descripe the exact ac voltage behaviour under different VAr compensating conditions. In fact, if the ac system Qac/V or Qac/Pdc demand characteristics are changed, different voltage stability properties would be obtained even if the SCR is kept the same.

AC Voltage Stabilization

Starting form those very reasons for ac voltage instability, it is possible to arrive to the effective solutions for such a problem.

A first, obvious and classical solution would be to increase the short circuit level at the ac/dc interconnection point. Synchronous condensers have been used in the past for such a purpose. However, they proved to be uneconomic, have high losses, and suffer from slow response compared to other static techniques. They can also deteriorate the overall ac/dc performance due to their inertial oscillations following system disturbances. The voltage stability factor for this case will be similar to that with SCR = 3.5.

On the other hand, regulated reactive power compensation can be achieved by means of static VAr compensators (SVC), such as thyristor controlled reactors, thyristor switched capacitors, or a combination of both. These SVC can form a part of the shunt capacitors Bc at the dc converter terminal. In this case the incremental change of reactive power of the SVC to the ac voltage change ($\Delta Qs/\Delta V$) can be made to be positive in the complete range of Pdc. The combined SVC and HVDC converter reactive power to voltage incremental change ($\Delta Qs+\Delta Qd)/\Delta V$ is as shown in Fig. 4(b). Since the SVC is assumed to have the appropriate rating (0.35 pu) to fully control the ac voltage under all steady state loading and transient conditions, the instability problem is eliminated as shown by the voltage stability factor in Fig. 3 (curve c).

A third, and most reliable and economic solution, is to regulate the reactive power consumed by the dc converter Qd in response to ac voltage variations. This can be realized by a localized ac voltage controller acting directly on the converter firing (or extinction) angle. As the ac voltage increases, for example, a high firing (or extinction) angle order is produced by the voltage regulator and overrides the signal from the dc master controller. Thereby, the dc voltage is temporarily reduced and consequently Qd increases to limit that overvoltage.

In other words, the HVDC converter is made to act in a similar manner to a thyristor controlled reactor SVC type. This, however, necessiates that the dc converter valves and their damping and cooling circuits are designed to accommodate the operation at high firing angles. The additional incremental investment in the dc converter required for such application, however, can be only a fraction of the total capital and operational costs associated with the other solutions. By this technique, the ratio $\Delta Qd/\Delta V$ is positive as shown in Fig. 4(c). Voltage instability is considerably reduced and the VSF is as shown inFig. 3(d). It is interesting to note that under this operating mode with SCR = 2.4 the overall system has a stabilized performance almost identical to the stiff system with SCR = 3.5. Therefore, temporary overvoltages expected in this case with the weak ac system would be in the same level as those for the stiff system. This will be demonstrated in the next sections.

AC VOLTAGE REGULATION BY HVDC CONVERTER CONTROLS

In order to establish the overall control strategy to simultaneously limit temporary overvoltages and enhance the performance of the dc system during and after fault conditions, the principles of ac voltage control method by the HVDC converter are first focused. A simple case is examined where the control action made by the HVDC converter (whether in rectifier or inverter operation) can be explained. For this purpose, a complete dynamic non-linear model for the full ac/dc systems is used for simulating the exact time response of the overall system. The digital simulations have been performed by means of the BBC Power System Simulation Programs where comprehensive fundamental frequency system models are utilized [7,8].

A capacitor bank (0.175 pu) is assumed to be switched on while the HVDC is operating at 100% load: This excessive amount of reactive power at the interconnecting bus can be effectively compensated by the reactive power absorbion of the HVDC converter if the latter is properly controlled for this purpose. As shown by the fundamental frequency digital simulation in Fig. 5.a, due to the switching on of capacitors in the weak ac system, temporary overvoltage is produced with a peak of 11%. However by advancing the firing angle α (as shown in Fig. 5.b) the reactive power absorbed by the dc converter is increased (Fig. 5.c) and the ac voltage is controlled back to 1.0 pu.

The same system has been modeled in the BBC HVDC simulator but with the full representation of filter banks and ac system sequence impedances and saturtion effects and employing a scaled thyristor valves and actual controllers. The transient behaviour of the 3-phase ac voltage during switching "on" the reactive power unit with the voltage controller in operation is as shown by the traces of Fig. 6.
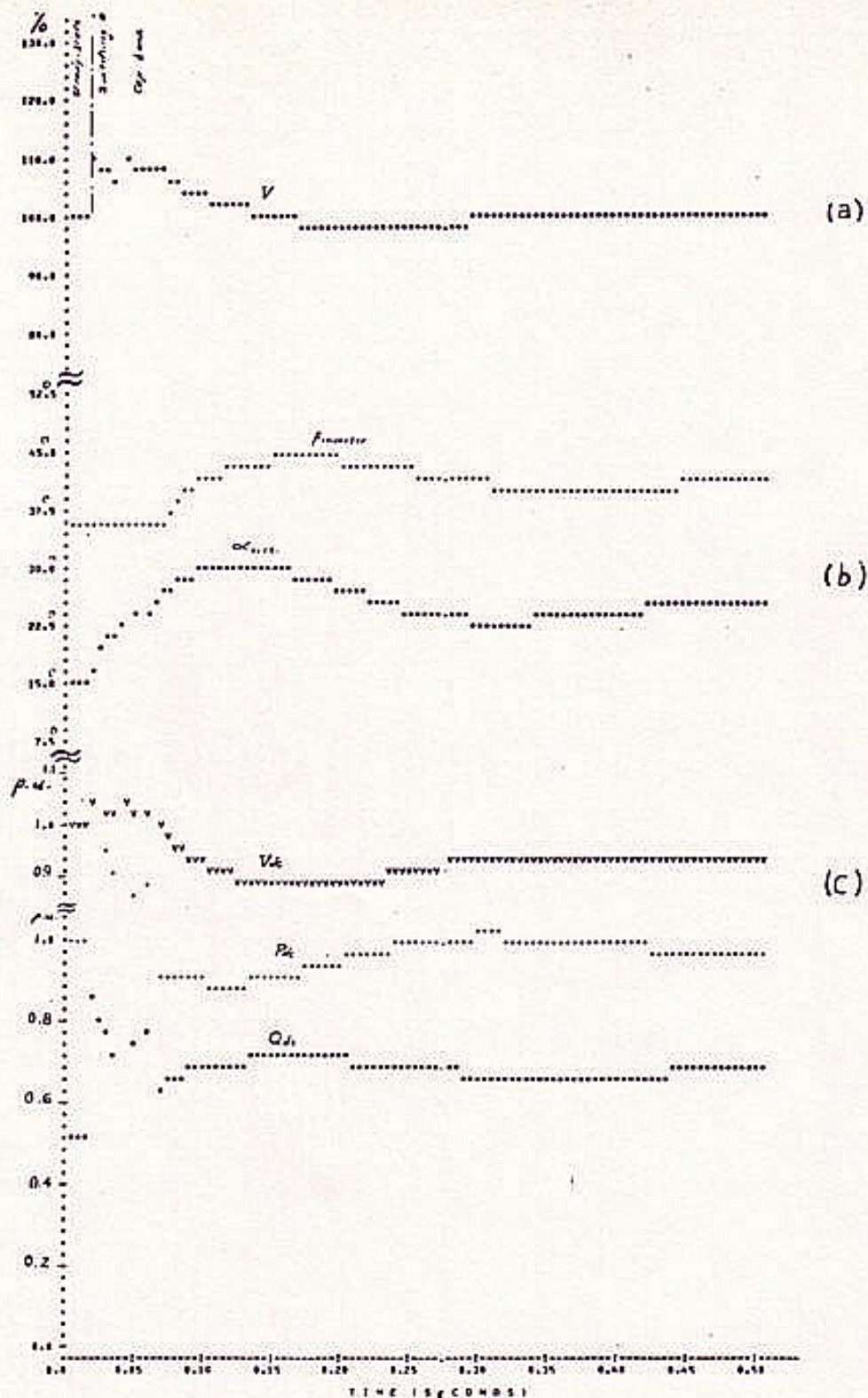
Fig. 5. Switching on a 0.175 pu capacitor bank at the dc terminal with ac voltage control mode of HVDC converters
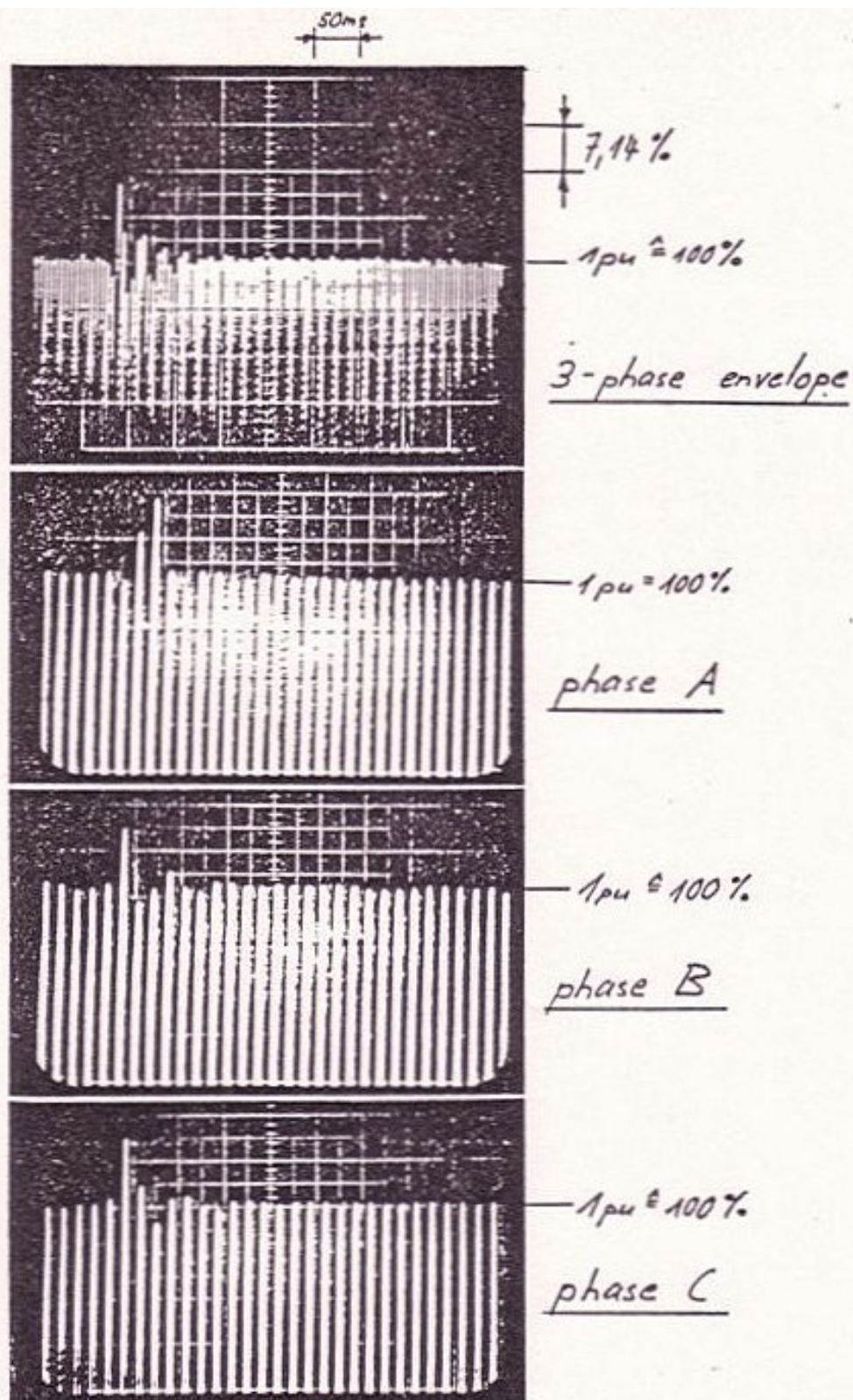
Fig. 6. Transient 3-phase voltage for switching on a 0.175 pu capacitor bank with HVDC ac voltage controller

The evident match between the results obtained by digital and analogue simulations in Figs. 5 and 6 respectively, clearly demonstrates the viability and effectiveness of the proposed technique.

Description of Basic Controls

It is now a common practice to use an HVDC converter terminal to help stabilize the interconnected ac system. Primarily, this is achieved by modulating the dc power, through the dc power order, in accordance with the ac system frequency variations. The oscillations - or modulations - in this case are known as "inertial oscillations" and are characterized by slow frequency (1-2 Hz). A similar action, as mentioned before, can be exerted but to affect the reactive power absorption and consequently controlling the ac voltage adjacent to the HVDC terminal. This control mode, however, is characterized by the relatively fast voltage oscillations compared to the system frequency oscillations. Under this condition an HVDC converter can be looked upon as a static VAr compensator with a rating ultimately equals the full MVA rating of its converter transformer. That is because a dc converter absorbs reactive power according to:

$$Qdc = Vdc \cdot Idc \cdot \tan \phi \tag{1}$$

where

$$\cos \phi \approx Vdc(pu) / Vac(pu) \tag{2}$$

and

$$Vdc(pu) = Vac(pu) \cdot \cos\alpha - Rc \cdot Idc(pu) \tag{3}$$

Therefore, by systematically changing the dc voltage Vdc, through firing (or extinction) angle α controllers, the reactive power Qdc consumed by the converter will be highly altered. When the HVDC converter is of a rating comparable to the ac system short circuit capacity (i.e. at low SCR), changing the Qdc can have an appreciable impact on the reactive power balance at the ac/dc interconnecting point and can consequently control the ac voltage. This control action is established in a fast and smooth manner in order to be effective in limiting for example any temporary overvoltages on the interconnected ac system.

The control scheme of an HVDC converter, in this case, is as shown in Fig. 7. During normal operation the convertr operates in either constant current mode (rectifier) or constant extinction angle mode (inverter). When the ac terminal voltage experiences any deviation from its set value, the output of the ac voltage regulator overrides other outputs. Produced new thyristors firing angle will immediately change the amount of reactive power absorbed by the dc terminal in such a way to control the ac voltage to its pre-set value. During this process, the other HVDC converter terminal will automatically take up the dc current control. Both HVDC terminals will then be running at comperative firing and extinction angles and consequently drawing the same order of magnitude of reactive powers. This, however, should not be of real concern since the dominant control action is to correct the voltage on the weaker ac side of the dc converter terminals and, therefore, the impact on the other stiffer side is minimum. Also, in the case when the dc link is connected in parallel with other ac lines, it is usually the case when a temporary overvoltage occurs at one point, simultaneous overvoltages with different magnitudes appear at other points, in the interconnected system. Therefore, changing the reactive power absorbed by the dc at both ends will be highly beneficial.

To accommodate for slower voltage variations and to keep the operating dc voltage close to its nominal value, coordination with switched VAr units (e.g. capacitors and filter banks) is necessary. This is illustrated in Fig. 8 for different dc power levels. For this purpose the controllers, integrated in the micro-processor based converter controls, must possess a hysteresis type characterstics to avoid undeterministic switching positions.

Control Strategy

The possible strategy to limit ac side overvoltages can now be set to be governed by the following criteria:

1. HVDC converter voltage controller is actuated if dynamic overvoltage exceeds a pre-set value.

   This will temporarily increase the converter firing angle (in case of rectifier) or extinction angle (in case of inverter). Such a control action is a continuous (smooth) variation of converter reactive power. Under these conditions, the high inverter extinction angles will always ensure a reliable dc operation in the weak ac system without the risk of commutation failures.

2. When a low dc voltage lasts for a pre-set time limit or if dynamic overvoltages persist for another pre-set time release signal for sequential switching operations for reactive power units. These switching actions are used primarily to ensure operation close to the nominal dc voltage and to supplement the controls to completely limit dynamic overvoltages.
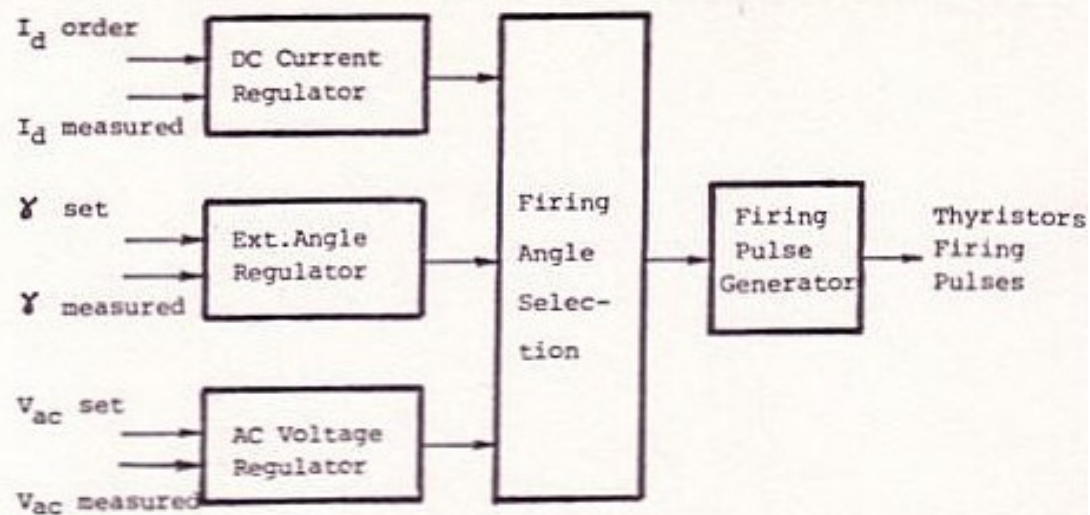
Fig. 7. Simplified diagram for proposed control scheme of an HVDC converter
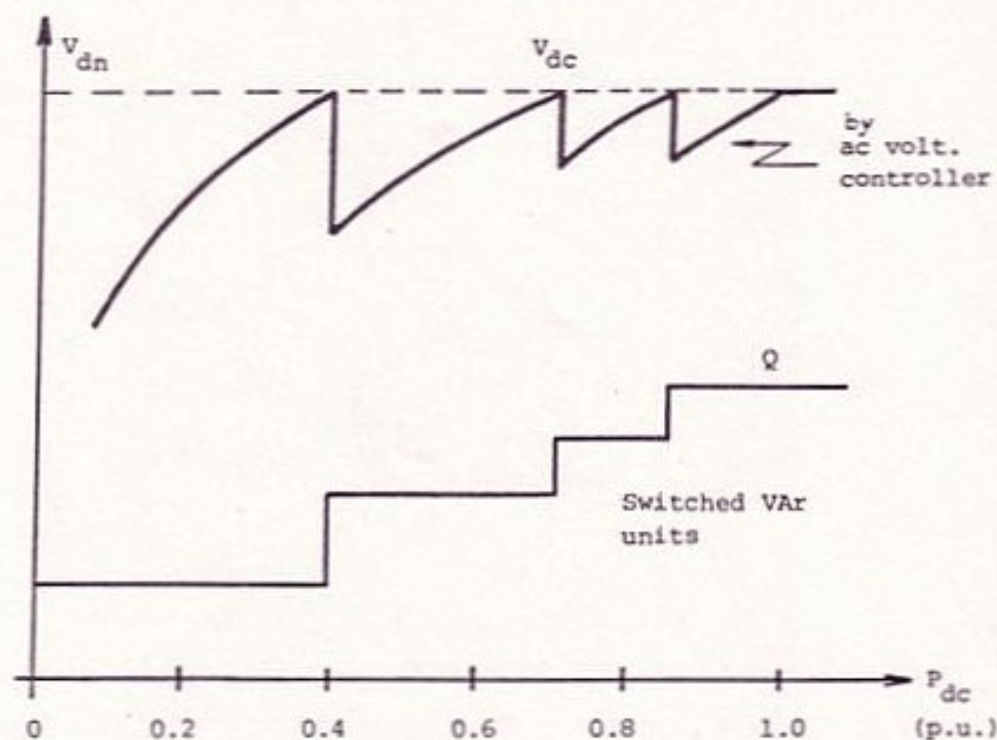

Fig. 8. Coordination between ac voltage controller and switched VAr units of an HVDC converter terminal

3. Static reactive power units (filters, capacitor banks, reactors) can be sequentially switched on or off according to the transmitted HVDC power level.

4. When ac voltages at the HVDC converter considerably drops, thus indicating a short circuit fault nearby the bus; capacitor banks are switched off or reactors are switched on in anticipation of high recovery overvoltage. Switching back these VAr units will follow criterion 3 and the smoothing action in between will be accomplished by means of criterion 1.

5. Under all conditions a minimum number of ac filter groups is left "on" for adequate HVDC restart.

TRANSIENT PERFORMANCE OF PROPOSED TECHNIQUE

Results of HVDC simulator studies are presented to illustrate the transient recovery process of the HVDC scheme following various faults at either one of its terminals.

A 3-phase short circuit fault is simulated on one ac line terminated at the HVDC rectifier terminal. The fault is assumed to be cleared in 6 cycles by opening the ac line without reclosing. The pre-fault short circuit ratio is 2.4 and after fault clearing it is 1.6.

Two control strategies - which constitute the major elements of the voltage control strategy explained in the previous section - are separately examined.

First, sequential switching of reactive power units (shunt capacitor banks and a filter in this case) is utilized. When the low ac voltage at the HVDC terminal is detected, all switchable capacitor banks and a filter (total 0.7 pu) are switched off (4 cycles after fault initiation). One filter bank is left for appropriate dc restart. The HVDC is blocked in one cycle and de-blocked in two cycles after fault clearing. High overvoltage is experienced after clearing the fault with a peak of 1.7 pu (Fig. 9). Following the dc power ramping, the filter and capacitor banks are sequentially switched back on. When the dc scheme is, however, allowed to continue firing instead of being blocked during the fault period, the results are as shown in Fig. 10. Without switching of any of the reactive power units, the HVDC scheme is able to first limit the recovery overvoltage (first peak is 1.25 pu) and second, to successfully ramp back to its full operation. This is achieved by the fast control action of the ac voltage regulator acting on the rectifier firing angle in this case. As shown in Fig. 10, the ac voltage magnitude is effectively and quickly controlled back to its prefault 1.0 pu value.
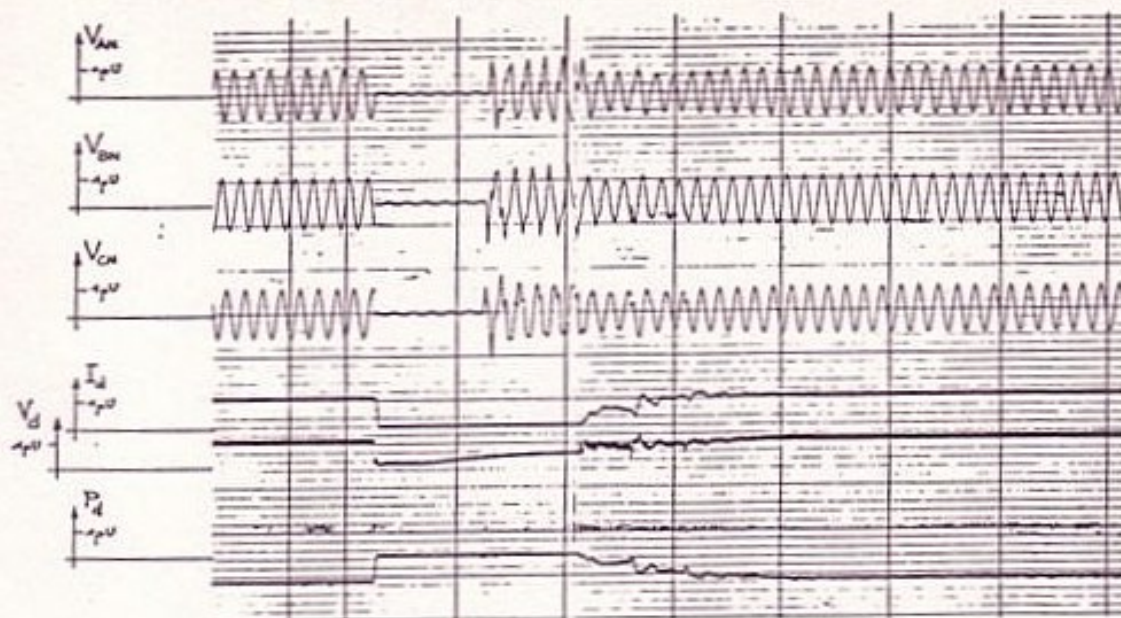
Fig. 9. System transient response for ac line 3-phase short circuit near rectifier cleared in 6 cycles by opening the line. Effective SCR = 1.6. With sequential switching of reactive power units
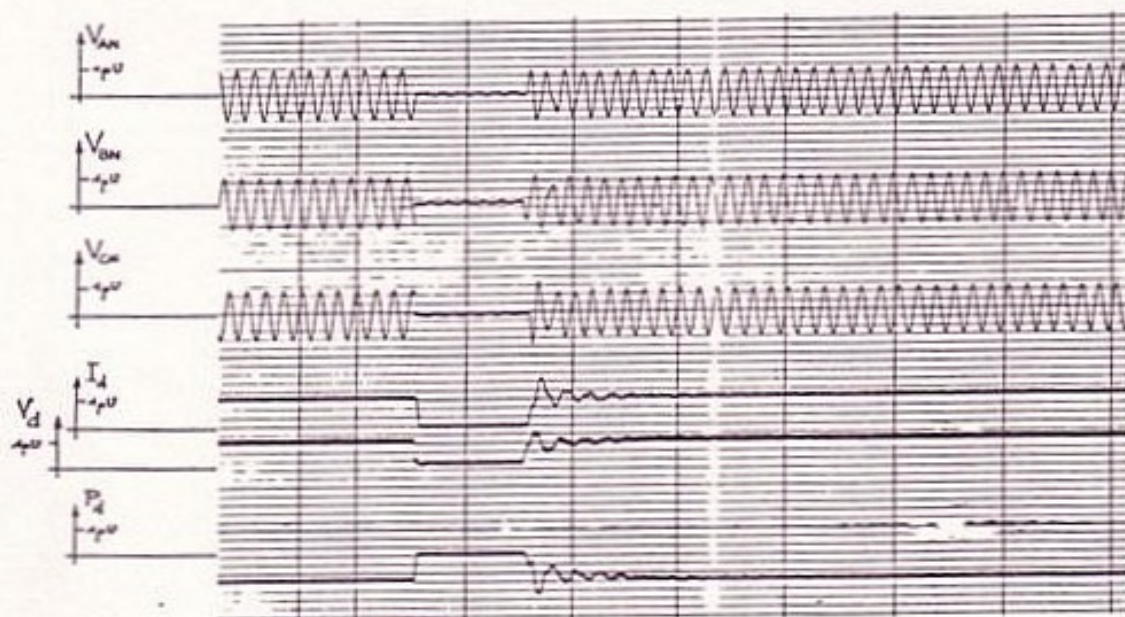

Fig. 10. System transient response for ac line 3-phase short circuit near rectifier cleared in 6 cycles by opening the line. Effective SCR = 1.6. With HVDC ac voltage controller. No capacitor switchings

Of course, when this control action is coordinated together with the switching operations of the reactive power units, the results would be significantly further improved due to the combined effects.

Other severe fault conditions have also been studied when the dc terminal is operating in either rectifier or inverter mode. When the proposed ac voltage control technique is adopted, the overall system transient response was similar to that shown in Fig. 10.

COMPARISON WITH OTHER VAR CONTROL TECHNIQUES

So far, only the proposed technique for voltage and recovery control has been thoroughly discussed. To further demonstrate its technical merits, this technique is compared to other known methods for voltage or reactive power control; namely, static VAr compensators and synchronous condensers. The comparison is carried out by the aid of digital time simulations of the fundamental frequency behaviour for the comprehensive ac/dc system model.

The same system discussed before where original short circuit ratio at the ac/dc interconnection point is 2.4 is studied. Synchronous condensers of 0.7 pu rating are added at the HVDC terminal to replace the switched reactive power units. The synchronous condensers are assumed to have a total transient reactance of 35% and step-up transformers of reactance 15% on their own rating. This will contribute an additional short circuit capacity of 1.4 pu at the HVDC terminal, thus increasing the effective SCR to become 3.8. A 3-phase short circuit fault is simulated on the ac side of the dc converter station. The fault is assumed to be cleared in 7 cycles without any line tripping. During the fault the HVDC converter is blocked and is ramped back to its prefault operation after fault clearing as shown in Fig. 11. The ac terminal voltage Vac is as shown with a recovery peak overvoltage of 9%. However, following complete recovery of HVDC, voltage and power fluctuations of + 2% and + 0.12 pu respectively take place at the terminals of the synchronous condensers. This is primarily due to the rotor oscillations of the synchronous condenser on account of its inertia, following the disturbance.

If static VAr compensators, say thyristor controlled reactors TCR with rating 0.35 pu, are employed instead, the switched VAr units (capacitors in this case) are also utilized. Controls of the combined scheme are driven by the variations of both voltage and reactive power at the HVDC terminal. Similar to the previous case, the dc is blocked during the 3-phase short circuit and allowed to recover after fault clearing (Fig. 12.). During the fault period the TCR is forced to be fully conducting and capacitor and filter banks of 0.35 pu are switched off in order to reduce the recovery overvoltages. After fault clearing the peak dynamic overvoltage is 9.3%. The HVDC recovers (in about 100 ms) as well as the power flow on the ac lines to prefault operating conditions. As the dc power ramps up, the switched capacitor and filter banks are switched back on sequentially. The reactive power absorbed by the TCR is also shown in Fig. 12.
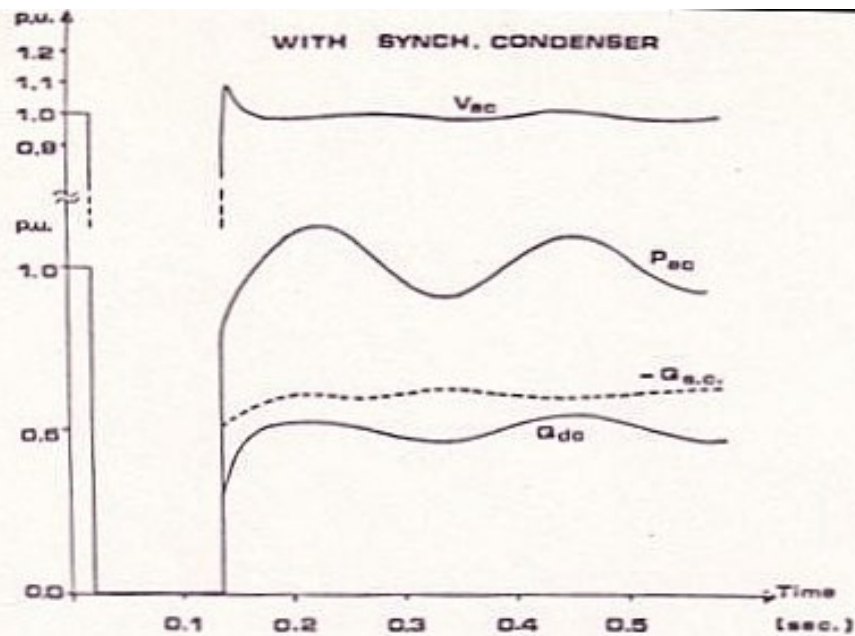
Fig. 11. System fundamental frequency response for 3-phase short circuit at HVDC converter terminal (7 cycles). With synchronous condensers (0.7 pu rating).
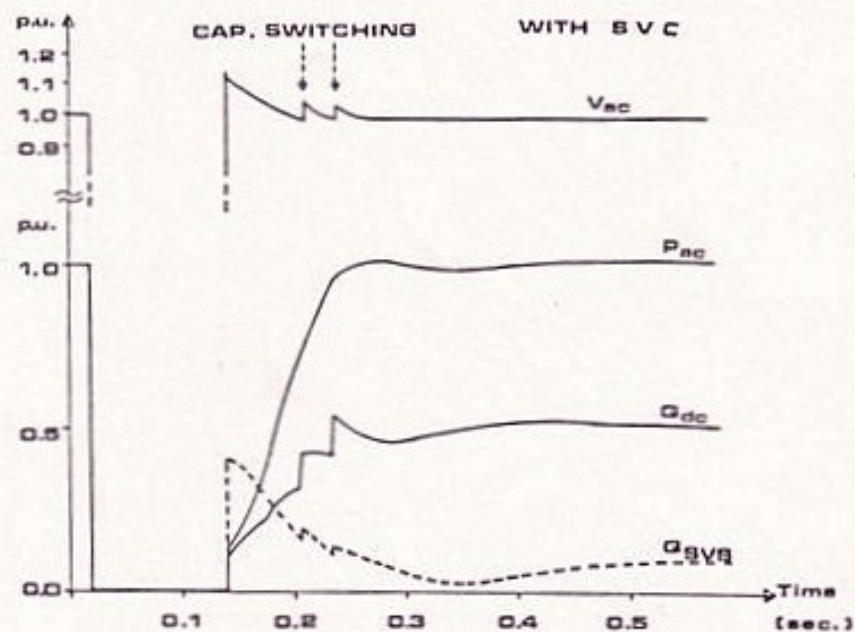

Fig. 12. System fundamental frequency response for 3-phase short circuit at HVDC converter terminal (7 cycles). With static VAr compensator (0.35 pu rating) and capacitor switchings
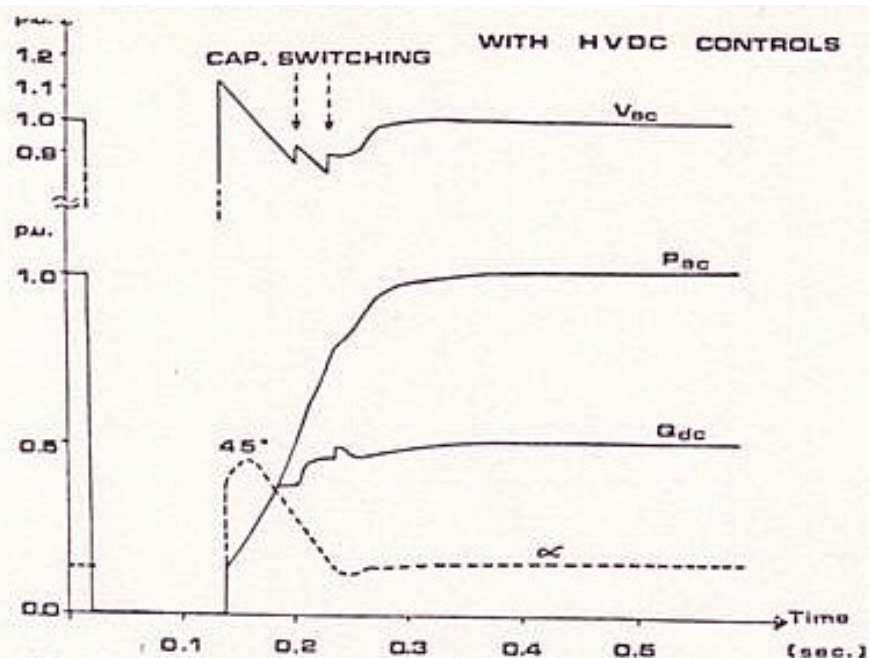
Fig. 13. System fundamental frequency response for 3-phase short circuit at HVDC converter teminal (7 cycles). With ac voltage controller of HVDC and capacitor switchings.

When the proposed technique of ac voltage control by the HVDC converter is used, the converter valves are kept conducting during the short circuit period. In anticipation of the high recovery temporary overvoltages, capacitor units of 0.525 pu are switched off and rectifier firing angle is kept high. The recovery overvoltage in this case is 12.5% but the ac voltge quickly drops as the HVDC is ramped back (Fig. 13). Following the dc power partial recovery accompanied by low ac and dc voltages the capacitor banks are sequentially switched back on. The ac voltage is controlled to 1.0 pu and the dc power recovers to pre-fault value as well as the power flow on the terminated ac lines. The dc voltage in this case is temporarily reduced to counteract the high dynamic overvoltage by increasing the reactive power absorption of the HVDC. This is achieved by means of the high firing angle $\propto$ shown in Fig. 13.

Results similar to those shown in Figs. 11-13 have also been obtaind during the course of the simulator studies.

It is worth noting that while the synchronous condenser produces oscillating power flows on the interconnected ac lines, such oscillations do not take place with static VAr compensation and voltage control methods. On the other hand the delay in the recovery of the dc terminal power after fault clearing on account of the temporary reduction of the dc voltage associated with the proposed technique is nearly isignificant. Compared to the case with static VAr compensators, the delay is only in the order of 1~2 cycles. Also when comparing the overall system losses, however, the voltage regulation technique by the HVDC converter controls proved to be economically attractive. On account of the relatively high losses associated with synchronous condensers and thyristor controlled reactors as well as their step down transformers, when operated at full loads, considerable savings in overall system losses can be achieved even when the HVDC scheme is temporarily running at low dc voltage levels.

CONCLUSIONS

HVDC schemes need ac systems with not too low relative short circuit capacity (SCR) to allow operation without excessive overvolatges at the ac busbar and with good fault recovery performance. So far synchronous condensers were considered as the only means to enlarge ac short circuit capacity. The paper shows evidence, that static compensation methods can be utilized as well for apparent SCR increase.

Static VAr compensators have been used as second generation ac voltage control equipment. While more economic than synchronous condensers they still constitute some cost penalties. It has been demonstrated in this paper, that for a third generation of ac bus-voltage control at an HVDC station the converters in combination with ac filters and capacitor banks can be directly used, even in case of long distance HVDC transmission, resulting in cosiderable savings in overall terminal cost as well as losses.

Results obtained by HVDC simulator and digital programs have shown that the fault recovery performance of HVDC converters with pure static compensation schemes is satisfactory and can be even improved without physically increasing the SCR by synchronous condensers.

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