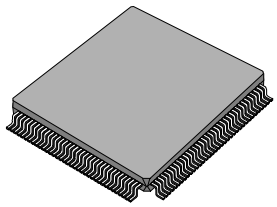
STA001

RF FRONT-END FOR DIGITAL RADIO

TARGET SPECIFICATION

- Single chip receiver for satellitedigital transmission
- Superheterodyne receiver with IF output
- High input intercept point, low mixer noise
- Receive RF frontend with 60dB IF gain control
- 15dB RF automatic gain control
- Integrated RF VCO
- Integrated IF VCO
- Integrated synthesizer
- I^2CBUS compatible programming interface
- Unregulated 2.7 V to 3.3V voltage supply
- Low cost external components

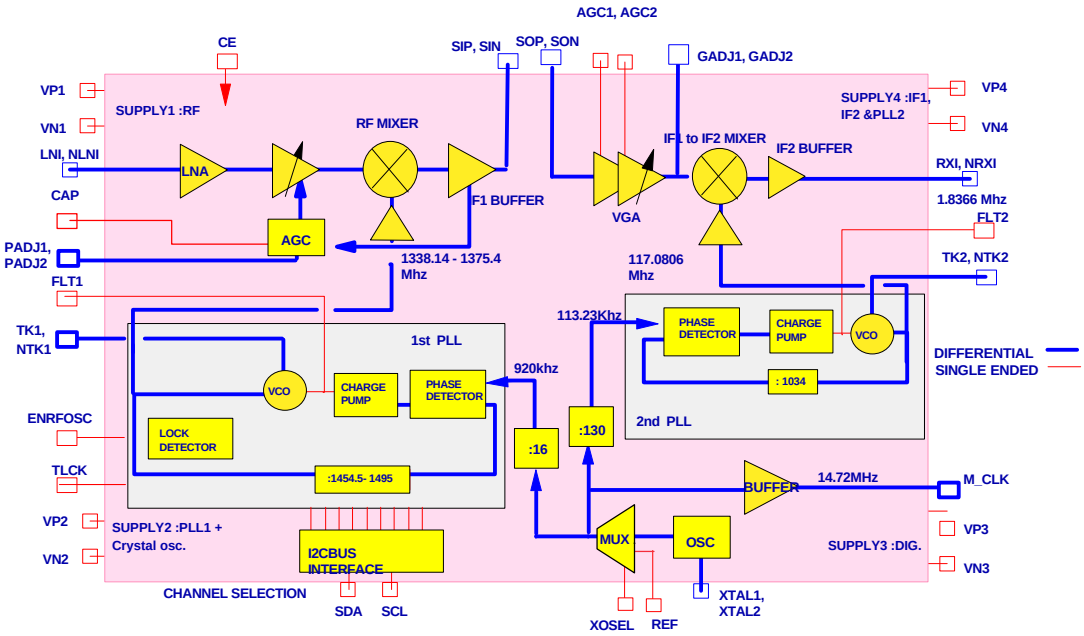


TQFP44

DESCRIPTION

The STA001 is an RF IC using STMicroelectronics HSB2 High Speed Bipolar Technology for one chip solution for the Starman digital satellite radio receiver.
The STA001 is assembled in a TQFP44 package. The frontend architecture is a double conversion receiver (see block diagram) .
The chip includes all the RF functions up to low IF and manages the signals to and from the baseband.

BLOCK DIAGRAM



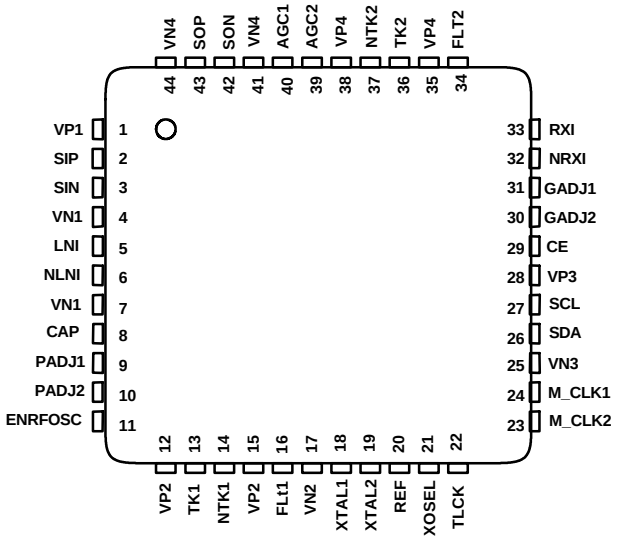
ABSOLUTE MAXIMUM RATINGS

Symb.	parameter	Value	units
T_{oper}	Operating temperature	-40 , +85	°C
T_{stg}	Storage temperature	-40 , +125	°C
V_{max}	Maximum voltage on any pin (with the exception of CE, SDA, SDL)	VP+0.3	V
V_{min}	Minimum voltage on any pin	GND-0.3	V
V_{maxi}	Maximum voltage on pins CE,SDA, SDL	VP+0.6	V
V_{pmax}	Minimum/Maximum power supply between $VP_{1,2,3,4}$ and $VN_{1,2,3,4}$	-0.3/5.5	V
V_{esd}	Electrostatic Discharge Voltage(ESD)	2	KV

OPERATING CONDITIONS

Symb.	parameter	Value	units
V_s	Operating voltage	2.7, 3.3	V
T_{jun}	Operating junction temperature(T_{ext}=25°, V_S=3V)	35	°C

PINS CONNECTION



PINS FUNCTION

N.	Name	Description	Notes
1	VP1	Positive supply 1	
2	SIP	SAW filter input connection	
3	SIN	SAW filter input connection	
4	VN1	Negative supply 1	
5	LNI	RF input	
6	NLNI	RF input	
7	VN1	Negative supply 1	
8	CAP	RF AGC loop external capacitor connection	
9	PADJ1	RF Peak level detection trimming connection 1	
10	PADJ2	RF Peak level detection trimming connection 1	
11	ENRFOSC	RF Oscillator enable	
12	VP2	Positive supply 2	
13	TK1	1st PLL tank connection 1	
14	NTK1	1st PLL tank connection 2	
15	VP2	Positive supply 2	
16	FLT1	1st PLL loop filter connection	
17	VN2	Negative supply 2	
18	XTAL1	Quartz oscillator connection 1	
19	XTAL2	Quartz oscillator connection 2	
20	REF	External optional TCXO input	
21	XOSEL	Internal/external XO selection	
22	TLCK	Lock detector output	

N.	Name	Description	Notes
23	M_CLK2	Master clock differential output 1	
24	M_CLK1	Master clock differential output 2	
25	VN3	Negative supply 3	
26	SDA	Data serial input	
27	SCL	Clock input	
28	VP3	Positive supply 3	
29	CE	Chip Enable	
30	GADJ2	IF bandwidth filter connection 2	
31	GADJ1	IF bandwidth filter connection 1	
32	NRXI	Low IF Signal output 2	
33	RXI	Low IF Signal output 1	
34	FLT2	2nd PLL loop filter connection	
35	VP4	Positive supply 4	
36	TK2	2nd PLL tank connection	
37	NTK2	2nd PLL tank connection	
38	VP4	Positive supply 4	
39	AGC2	VGA control pin 2	
40	AGC1	VGA control pin 1	
41	VN4	Negative supply 4	
42	SON	SAW filter output connection	
43	SOP	SAW filter output connection	
44	VN4	Negative supply 4	

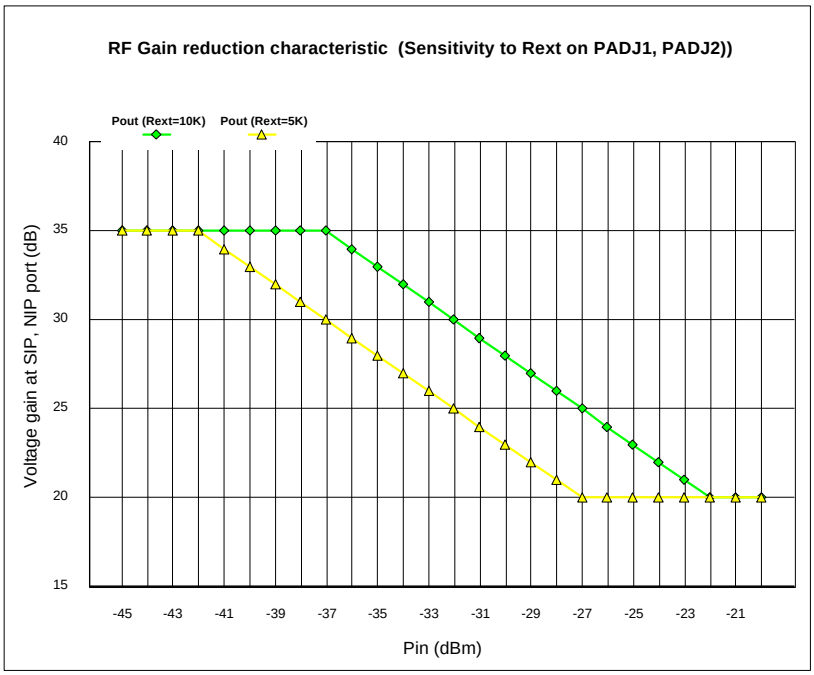
ELECTRICAL CHARACTERISTICS

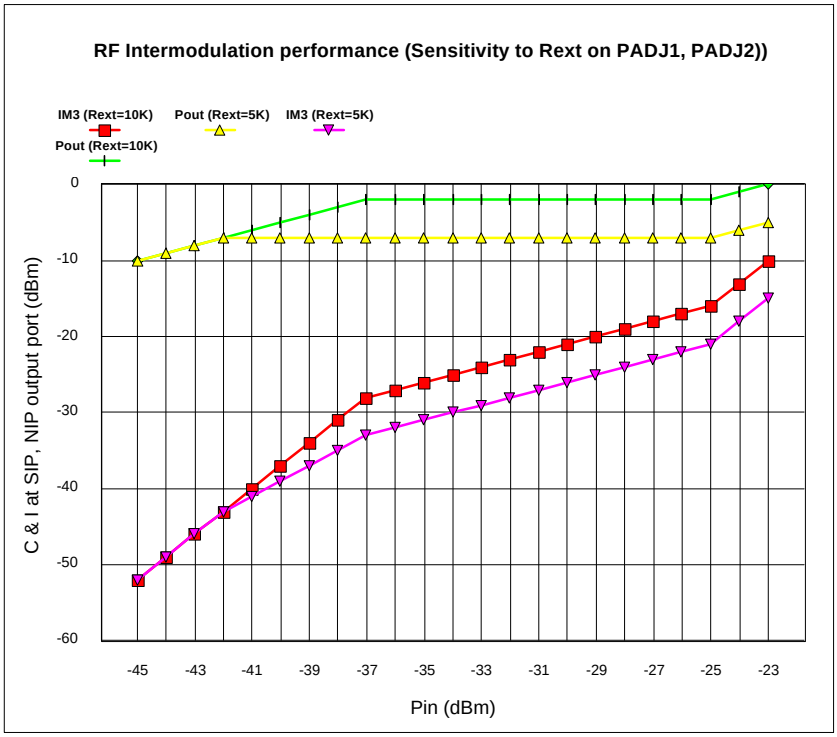
Supplies (T=25º, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
I_{CC1}	Current supplied by VP1	Powered circuits: LNA, RF mixer, IF buffer		15,8	19	mA
I_{CC2}	Current supplied by VP2	Powered circuits: RF pll, Crystal Oscillator. ENRFOSC=high (IC RF Osc. Enabled), XOSEL=high (IC XO Enabled)		9.6	12	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=high (IC XO Enabled)		3.2	4	mA
		ENRFOSC=high (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)		8.4	11	mA
		ENRFOSC=low (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)		2	2.5	mA
I_{CC3}	Current supplied by VP3	Powered circuits: Digital cells		11,8	15	mA
I_{CC4}	Current supplied by VP4	Powered circuits: VGA, IF mixer, output buffer, IF pll. V(AGC1)=V(AGC2)=1.2 (IF_{gain}=75dB)		10	13	mA
I_{TOT}	I_{CC1}+ I_{CC2}+ I_{CC3}+ I_{CC4}	ENRFOSC=high (IC RF Osc. Enabled), XOSEL=high (IC XO Enabled)		47.2	59	mA
		ENRFOSC=low (IC RF Osc. Disabled), XOSEL=high (IC XO Enabled)		40.8	51	mA
		ENRFOSC=high (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)		46	58	mA
		ENRFOSC=low (IC RF Osc. Enabled), XOSEL=low (IC XO Disabled)		39.6	49.5	mA
I_{TOTSB}	Standby I_{CC1}+ I_{CC2}+ I_{CC3}+ I_{CC4}	CE=GND			100	uA

Lna, RF mixer and IF1 BUFFER (T=25°, VP-VN=3V)

Symb.	Parameter	Test condition / notes	Min.	Typ.	Max.	Units
BW_i	Input signal BW		1452		1492	MHz
BW_o	Output signal BW		114		116,5	MHz
G_{Vmin}	Minimum Voltage Gain	R_L = 200Ω	17	20	23	dB
G_{Vmax}	Maximum Voltage Gain	R_L = 200Ω	33	35	37	dB
Z_i	Input impedance R || C	Balanced, LNI, NLNI pins		75 0.2		Ohm pF
Z_o	Output impedance	Balanced, SIP, SIN pins	41	50	59	Ohm
R_l	Input Return Loss	Input of LNA	7	14		dB
IIP3ol	Open RF AGC loop Input IP3	Gain = 35dB, Input of LNA	-26	-24		dBm
IIP3	Input IP3	R_{ext}=5K connected between PADJ1, PADJ2, Input of LNA	-20	-17		dBm
1 dB c.p.	Input 1 dB compression, open AGC loop	Gain = 35dB, Input of LNA	-35	-33		dBm
NF	Noise figure contribution	Gain = 35dB, R_s=50Ω, R_l=200Ω		5	7	dB
$IF1_{leak}$	LO1 to IF1 leakage			-29	-25	dBm
RF_{leak}	LO1 to RF leakage			-49	-30	dBm
V_{DC}	LNI, NLNI common mode DC voltage	AC coupled to the Balun	VP-1.4	VP-1.2	VP-1	V
V_{DC}	SIP, SIN common mode DC voltage	AC coupled to the SAW filter	VP-1.3	VP-1.1	VP-0.9	V
V_{DC}	PADJ1 PADJ2 CAP	R_{ext}=5K connected between PADJ1, PADJ2	VP-0.85 VP-0.78 VP-0.25	VP-0.7 VP-0.625	VP-0.55 VP-0.47 VP	V
τ_{AGC}	RF AGC loop time constant	C_{ext} =100nF connected on CAP	68	81	94	uS
P_{RF1}	RF Input power level at which RF gain starts decreasing (see next page graphs)	R_{ext}=5K, tolerance=±1%	-46	-42	-38	dBm
P_{RF2}	RF Input power level at which RF gain ends decreasing (see next page graphs)	R_{ext}=5K, tolerance=±1%	-32	-27	-22	dBm
G_{Vrange}	AGC gain range	R_{ext}=1K~10K	13	15	17	dB

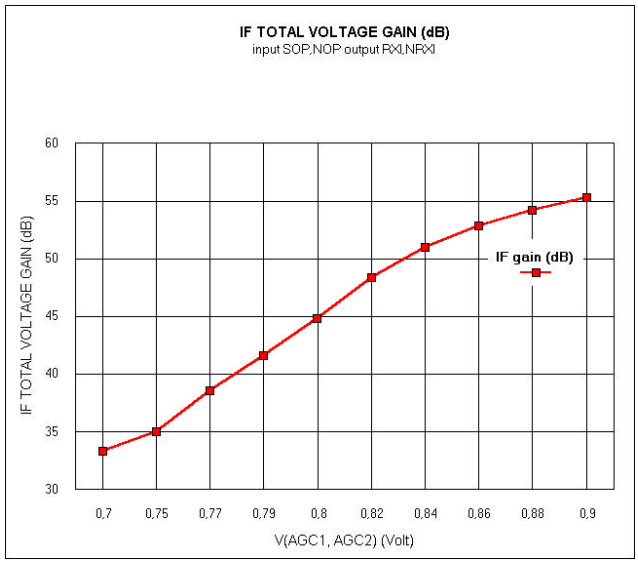


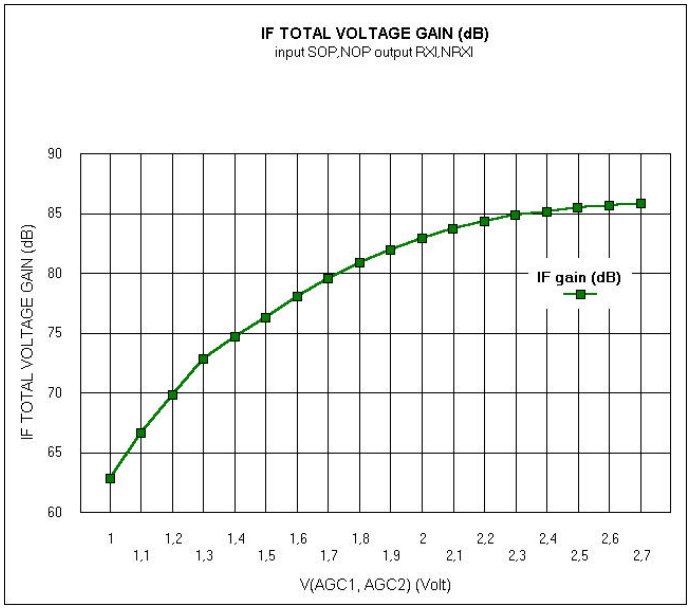


TYPICAL RF GAIN/P_{out}/IM3 vs INPUT POWER

IF VGA amplifier, IF mixer and output buffer (T=25º, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
BW_i	Input signal BW		114		116,5	MHz
BW_o	Output signal BW		0,6		3,1	MHz
G_{min}	Minimum gain	$V(AGC_{1,2})$=0V		32	37	dB
G_{max}	Maximum gain	$V(AGC_{1,2})$=3V	81	86		dB
I_{AGC}	Input current in AGC control pin				10	uA
Z_{AGC}	AGC pin input impedance		150	600		KOhm
NF	Noise figure contribution	Gain = 75dB, Rs=200Ω		7,5	10	dB
NF	Noise figure contribution	Gain = 49dB Rs=200Ω		24	27	dB
1dB c.p.	Input 1 dB compression point	Gain = 75dB	-68	-65		dBm
1dB c.p.	Input 1 dB compression point	Gain = 49dB	-42	-39		dBm
IIP3	Input IP3	Gain = 75dB	-59	-56		dBm
IIP3	Input IP3	Gain = 49dB	-33	-30		dBm
Z_{in}	Input impedance	Balanced, SOP, SON pins	42,5	50	57,5	Ohm
Z_{out}	Output impedance	Balanced, RXI, NRXI pins	150	200	250	Ohm
V_{out}	Output differential Voltage swing			1	1,5	V_{pp}
V_{DC}	SOP, SON common mode DC voltage	AC coupled to the SAW filter	VP-1.2	VP-1	VP-0.8	V
V_{DC}	RXI, NRXI common mode DC voltage		VP-1.6	VP-1.3	VP-1	V
V_{DC}	GADJ1, GADJ2 common mode DC voltage		VP-0.15	VP-0.12	VP-0.09	V
Z_{adj}	Gain adjustment pins impedance	Balanced, GADJ1, GADJ2 pins	650	800	950	Ohm
BB_{leak}	LO2 to BB leakage	Obtained using low pass filter at the output		-45	-30	dBm
$IF2_{leak}$	LO2 to IF2 leakage	Obtained with SAW filter connected to IF port		-44	-30	dBm
IM3	Third order IM product	$V_{out}=1V_{pp}$			-30	dBc





TYPICAL IF OVERALL GAINvs CONTROL VOLTAGE

Crystal oscillator (T=25°, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
f_{xtal1}	Quartz frequency	- Resonance mode: series - Using a 14.72		14,72		MHz
f_{xtal2}	Quartz frequency	- Resonance mode: series - using a 14.725 quartz		14,725		MHz
P_n	Phase noise	Δf = 1 KHz		-120	-118	dBc/Hz
V_{DC}	XTAL1, XTAL2 common mode DC voltage	XOSEL high	VP-1.1	VP-0.9	VP-0.7	V

PLLs, Synthesizers (T=25°, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
t_s	RF pll loop settling time	within 1 KHz final freq. Offset, by using the loop filter of Application board		1	10	ms
P_n	Total phase noise contribution	100Hz < Δf < 1.84Mhz, $Q_{rf\_tank} \geq 20$, $Q_{if\_tank} \geq 20$			2	deg_{rms}
f_{REF1}	RF pll comparation frequency			920		KHz
f_{REF2}	IF pll comparation frequency			113.23		KHz
P_{SP}	Spurious power level	RF pll, Δf_c=920KHz IF pll, Δf_c=113.23KHz			50 50	dBc dBc
N_{prog1}	RF PLL selectable division ratios	from REF1 to LO1, range covered by a 0.5 step, using a 14.72MHz quartz	1443 (first used 1454.5)		1506.5 (last used 1495)	
N_{prog2}	RF PLL selectable division ratios	from REF1 to LO1, range covered by a 0.5 step, using a 14.725MHz quartz	1443 (first used 1454)		1506.5 (last used 1494.5)	
N_{fix}	IF PLL fixed division ratios	from REF2 to LO2, 1 fixed +2 testing values	987	1034	1081	
N_{REF1}	REF1 division ratio	from Crystal oscillator to REF1		16		
N_{REF2}	REF2 division ratio	from Crystal oscillator to REF2		130		

RF VCO (T=25º, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
f_{LO1_1}	LO Freq. range	Using 14.72Mhz quartz	1338.14		1375.4	MHz
f_{LO1_2}	LO Freq. range	Using 14.725Mhz quartz	1338.134375		1375.407031	MHz
V_{FLT1}	Freq. control voltage range	Pin FLT1	VN + 0.2		VP - 0.2	V
P_n	Phase noise	@100 KHz @ (SIP, NIP pins), $Q_{rf\_tank} \geq 20$		-110	-108	dBc/Hz
V_{DC}	TK1, NTK1 DC voltage	ENRFOSC high	VP-1.3	VP-1.1	VP-0.9	V
Z_i	Input impedance R || C	Balanced, TK1, NTK1 pins		300 0.2		Ohm pF

IF VCO (T=25º, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
f_{LO2_1}	LO Freq.	Using a 14.72MHz quartz, Min. and Max. Values are optional fixed frequency usable for testing purposes.	111.76	117.08	122.4	MHz
f_{LO2_2}	LO Freq.	Using a 14.725MHz quartz, Min. and Max. Values are optional fixed frequency usable for testing purposes.	111.8	117.12	122.44	MHz
V_{FLT2}	Freq. control voltage range	FLT2 pin	VN + 0.2		VP - 0.2	V
P_n	Phase noise	@100KHz @ (RXI, NRXI pins), $Q_{if\_tank} \geq 20$		-115	-113	dBc/Hz

Digital interface to µP (SCL, SDA, TLCK) and XOSEL interface (T=25°, VP-VN =3V)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
V_{IH}	digital input signals	high	VP-1		VP	V
V_{IL}		low	VN		VN+1	V
I_{IH}	Input current High		10			uA
I_{IL}	Input current Low				-40	uA
Tt	Input edge transition				0.1	us/V
V_{OH}	digital output signals	high	VP-0.5		VP	V
V_{OL}		low	VN		VN+0.5	V
t_r	Rise time	Cl=5pF		0.4	0.6	us/V
t_f	Fall time	Cl=5pF		0.4	0.6	us/V
R_{in}	Input resistance		160K	190K	220K	Ohm
I_{max}	Maximum input current into SCL, SDA	During transient overvoltage condition			10	mA

Differential Digital interface(M_CLK1, M_CLK2) (T=25º, VP-VN =3V)

Symbol	Parameter	Test condition / notes	Min	Typ.	Max.	Units
V_{OH}	digital output signals, V(M_CLK1) - V(M_CLK2)	high		0.2		V
V_{OL}		low		-0.2		V
V_{DC}	M_CLK1, M_CLK2 common mode DC voltage		VP-1.1	VP-0.9	VP-0.7	V
t_r	Rise time	Cl=5pF each pin		10	12	ns
t_f	Fall time	Cl=5pF each pin		10	12	ns
Z_{out}	Output impedance	balanced		500	600	Ohm
f_{M_CLK1}	M_CLK frequency	Using a 14.72MHz quartz		14.72		MHz
f_{M_CLK2}	M_CLK frequency	Using a 14.725MHz quartz		14.725		MHz

Additional digital interface(CE) (T=25º, VP-VN =3V)
(low=GND, high=VP)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
V_{IH}	digital input signals	high	VN+1.8			V
V_{IL}		low			VN+1.3	V
t_r	CE power up time				2	us
t_f	CE power down time				6	us
I_{max}	Maximum input current into CE	During transient overvoltage condition			10	mA

XOsel, CE, TLCK, ENRFOSC truth table
(low=GND, high=VP)

PIN	TYPE	Level	result
CE	input	high	Chip enabled
		low	Chip disabled
XOSEL	input	high	Internal Crystal oscillator selected
		low	External TCXO connected on REF selected
ENRFOSC	input	high	Internal RF oscillator selected
		low	External RF oscillator connected on TK1, NTK1 pins
TLCK	output	high	Synth. locked
		low	Synth. unlocked

Additional optional interface information (REF)

Symb.	Parameter	Test condition / notes	Min	Typ.	Max.	Units
P_{REF}	Optional testing external reference clock connected on REF power	It must be AC coupled to REF, XOSEL low	-2	0		dBm
V_{DC}	REF DC voltage	XOSEL low	VP-1.1	VP-0.9	VP-0.7	V
R_{in}	Input resistance	XOSEL low	60K	70K	80K	Ohm

I²C BUS INTERFACE

Data transmission from microprocessor to the STA001 takes place through the 2 wires I²C BUS interface, consisting of the two lines SDA and SCL (pull-up resistors to positive supply voltage must be connected to SDA and SCL).

Data Validity

The data on the SDA line must be stable during the high period of the clock. The HIGH to LOW state of the data line can only change when the clock signal on the SCL line is LOW.

Start and Stop conditions

A start condition is a HIGH to LOW transition of the SDA line while SCL is HIGH. The stop condition is a LOW to HIGH transition of the SDA line while SCL is HIGH.

Byte format

Every byte transferred on the SDA line must contains bits. Each byte must be followed by an acknowledge bit. The MSB is transferred first.

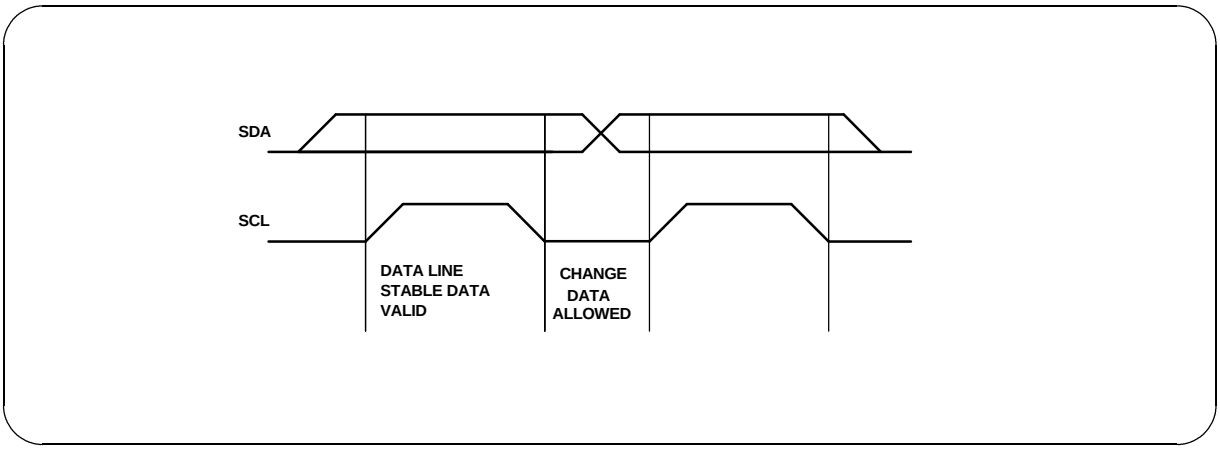
Acknowledge

The master (µP) puts a resistive HIGH level on the SDA line during the acknowledge clock pulse. The peripheral (STA001) that acknowledges has to pull-down (LOW) the SDA line during the clock pulse.
The STA001 which has been addressed has to generate an acknowledge after the reception of each byte, otherwise the SDA line remains at at the HIGH level during the ninth clock pulse time. In this case the µP can generate the STOP information in order to abort the transfer.

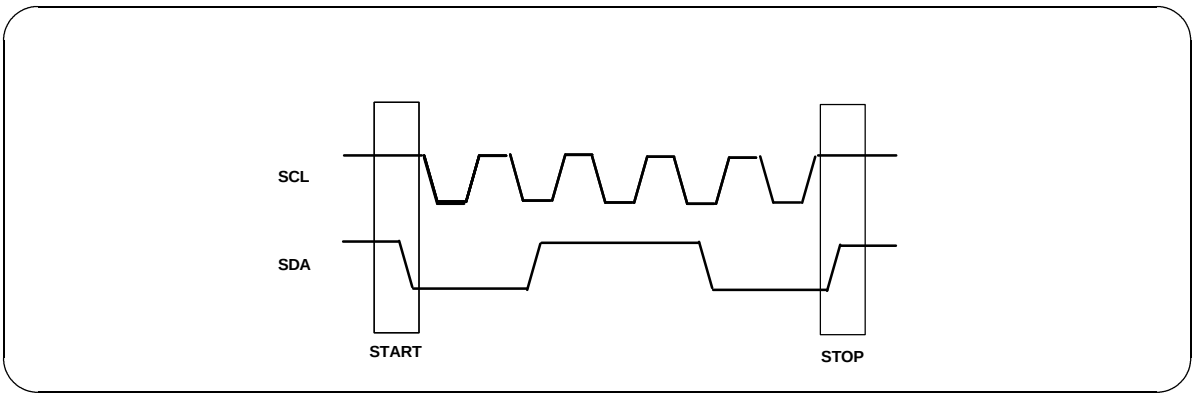
Transmission without acknwoledge

Avoiding to detect the acknowlegde of the STA001, the µP can use a simpler transmission: simply it waits one clock period without checking the STA001 acknowledging, and sends the new data.
This approach of course is less protected from misworking.

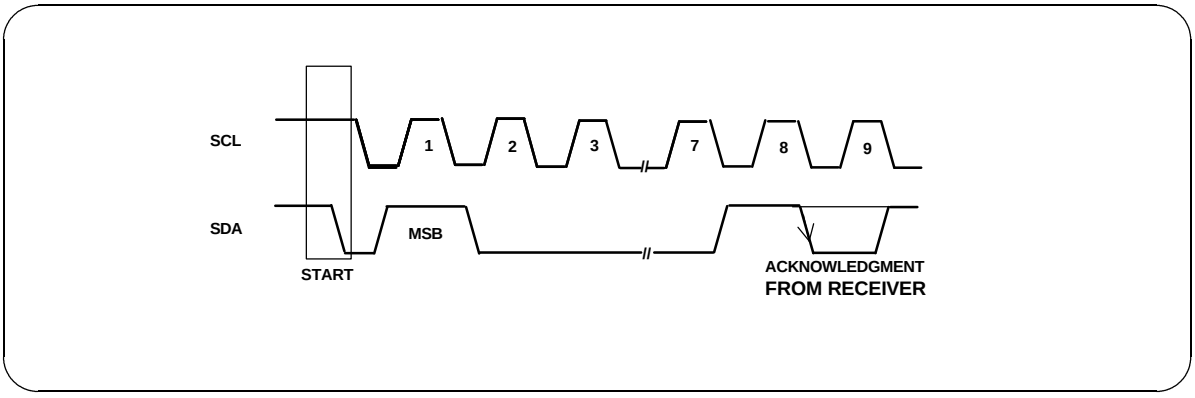
Data Validity on the I^2CBUS:



Timing Diagram of theI^2CBUS:

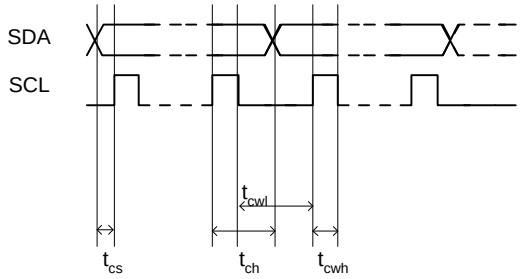


Acknowledge on theI^2CBUS:



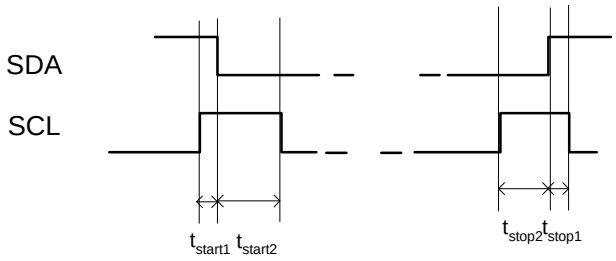
Timing specification

Data and clock



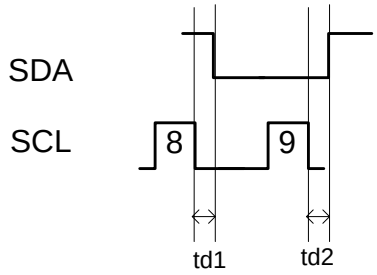
Symbol	Parameter	Minimum time (ns)
t_{cs}	Data to clock set up time	100
t_{ch}	Data to clock hold time	50
t_{cwh}	Clock pulse width high	100
t_{cwl}	Clock pulse width low	100

Start and stop



Symbol	Parameter	Minimum time (ns)
$Tstart_{1,2}$	Clock to data start time	100
$Tstop_{1,2}$	Data to clock down stop time	100

Ack



Symbol	Parameter	Maximum time (ns)
t_{d1}	Ack begin delay	200
t_{d2}	Ack end delay	200

SOFTWARE SPECIFICATION

Interface protocol

The interface protocol comprises:

- A start condition (S)
- A chip address byte
- A two data bytes
- A stop condition (P)

MSB			chip address					LSB	MSB				1st data byte					LSB	MSB				2nd data byte					LSB		
S	1	1	0	0	0	0	0	0	ack	1	D6	D5	D4	D3	D2	D1	D0	ack	0	D6	D5	D4	D3	D2	D1	D0	ack	P

ack = Acknowledge
S = Start
P = Stop

"Byte by byte" option

A "byte by byte" programming mode is also possible when there is no need to use both data bytes to program the chip (for example during the setup of 2nd PLL).
To use this feature remember that first bit of both data bytes is reserved to chose the destination of the remaining 7 bits.

MSB			chip address					LSB	MSB					data byte				LSB		
S	1	1	0	0	0	0	0	0	ack	K	D6	D5	D4	D3	D2	D1	D0	ack	P

ack = Acknowledge
S = Start
P = Stop
K= destination of the remaining7bit:

K=1 the data byte has the same function of the 1st data byte in the normal programming mode.
K=0 the data byte has the same function of the 2nd data byte in the normal programming mode.

First data byte selection table (selection of synthesizer channel) using á4.72Mhz quartz

MSB						LSB	RF LO freq. selected	Units	Division ratio selected on synthesizer	Notes
D6	D5	D4	D3	D2	D1	D0			from REF1 to LO1	
0	0	0	0	1	1	0	1324.8+6*0.46 (1327.56)	MHz	1443	Lowest selectable freq.
0	0	0	0	1	1	1	1324.8+7*0.46	MHz	1443.5	
0	0	0	1	0	0	0	1324.8 + 8*0.46	MHz	1444	
-	-	-	-	-	-	-				
0	0	1	1	1	0	1	1338.14	MHz	1454.5	first used freq.
-	-	-	-	-	-	-	1324.8 + N*0.46 N=(D6..D0) represented decimal number	MHz	1440 + N*0.5	general freq. generation rule
1	1	0	1	1	1	0	1375.4	MHz	1495	Last used freq.
-	-	-	-	-	-	-				
1	1	1	1	1	1	1	1383.22	MHz	1503.5	
0	0	0	0	0	0	0	1383.68	MHz	1504	
-	-	-	-	-	-	-				
0	0	0	0	1	0	1	1324.8+133*0.46 (1385.98)	MHz	1506.5	Highest selectable freq.
1	0	0	0	1	0	1	1356.54	MHz	1474.5	Startup presetted data

First data byte selection table (selection of synthesizer channel) using á4.725Mhz quartz

MSB						LSB	RF LO freq. selected	Units	Division ratio selected on synthesizer	Notes
D6	D5	D4	D3	D2	D1	D0			from REF1 to LO1	
0	0	0	0	1	1	0	1325.25 +6*0.46015625 (1328.010938)	MHz	1443	Lowest selectable freq.
0	0	0	0	1	1	1	1325.25 +7*0.46015625	MHz	1443.5	
0	0	0	1	0	0	0	1325.25+ 8*0.46015625	MHz	1444	
-	-	-	-	-	-	-				
0	0	1	1	1	0	0	1338.134375	MHz	1454	first used freq.
-	-	-	-	-	-	-	1325.25+ N*0.46015625 N=(D6..D0) represented decimal number	MHz	1440 + N*0.5	general freq. generation rule
1	1	0	1	1	0	1	1375.407031	MHz	1494.5	Last used freq.
-	-	-	-	-	-	-				
1	1	1	1	1	1	0	1383.229688	MHz	1503	
1	1	1	1	1	1	1	1383.689844	MHz	1503.5	
-	-	-	-	-	-	-				
0	0	0	0	1	0	1	1325.25 +133*0.46015625 (1386.450781)	MHz	1506.5	Highest selectable freq.
1	0	0	0	1	0	1	1357.000781	MHz	1474.5	Startup presetted data

Second data byte selection table (LOCK test on both pll, dividers test and IF pll test)

MSB						LSB	Working mode	Notes
D6	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
0	0	0	0	0	0	0	Lock test on RF pll	lock flag to be tested: TLCK; Startup presetted data
0	0	0	0	1	0	0	Lock test on IF pll	lock flag to be tested: TLCK
0	0	0	0	0	0	1	Lock test on RF and IF pll	lock flag to be tested: TLCK
0	0	1	0	0	1	0	First pll programmable divider test	output freq. divided by 16 available on TLCK
0	0	1	1	0	1	0	First pll reference divider test	output freq. divided by 8 available on TLCK
0	0	1	0	1	1	0	Second pll fixed divider test	output freq. divided by 2 available on TLCK
0	0	1	1	1	1	0	Second pll reference divider test	output freq. available on TLCK
1	0	0	0	0	0	0	Test frequency on IF pll divider by 1034	Division ratio changed to 987
1	1	0	0	0	0	0	Test frequency on IF pll divider by 1034	Division ratio changed to 1081

FUNCTIONAL DESCRIPTION

Receiver chain

The receiver chain transforms the RF frequency signals to an IF signal at 1.84 MHz Carrier directly usable by the Channel decoder.

In front of the STA001 IC is placed an external LNA and a bandpass filter; the bandpass filter limitates the input bandwidth and guarantees a suitable rejection to the image frequency.

The input stage is a LNA working in the 1452-1492 MHz band. A second gain stage after the LNA has a variable gain suitable for high level interference situations.

The interference level is measured by a power detector located into the IF1 Buffer and compared with a reference level adjustable with an external resistive trimmer connected between PADJ1, PADJ2 pins (see application circuit). An error amplifier regulates the RF gain comparing the 2 values.

The value of the resistor should be fixed depending on wanted IM3 performances.

By connecting R_{ext}=10K, for example, an IM3 of 25dBc about is mantained by the receiver in condition of strong interference (see graph on page 7); an increase [decrease] of 2dBc IM3 about is obtained for each 10% decrease [increase] of R_{ext}.

By this approach it's possible to privilege IC noise or interference performance.

The RF signal is downconverted, using an active mixer, to a first IF of 115.244 MHz.

The first LO is tunable with a frequency step of 460KHz.

An IF variable gain amplifier guarantees a 60 dB typical gain range.

Using pins GADJ1, GADJ2, the output RX signal level can be lowered to desired value by a resistive trimmer.

Moreover, using static connection on AGC1, AGC2 pins, the IF chain can be configured to have a fixed gain by fixing statically control voltages (i.e. V(AGC1)=VCC and V(AGC2)=GND), and by trimming the gain through connecting an external resistor between GADJ1 and GADJ2. By using an 800 Ohm resistor connected between GADJ1 and GADJ2, for example, a typical 56dBs IF static gain is obtained.

The first IF signal, having a bandwidth of 2.5 MHz, shaped by an external SAW filter, is downconverted to a second IF of 1.84 MHz.

A clock at 14.72 MHz is available at two differential pins to be used from the baseband.

Synthesizers, PLL, charge pump and VCOs

The first Voltage controlled Oscillator is controlled by an integrated PLL and it's able to cover a frequency range of 37 MHz with a step size of 460KHz.

The second Voltage controlled oscillator produces a fixed 117.08MHz frequency controlled by a second integrated PLL. Moreover, 2nd pll is able to select 2 other fixed frequencies, i.e. 111.76MHz and 122.4MHz, suitable for application test.

The other components of the first PLL synthesizer are a low frequency programmable divider and a dual modulus prescaler; a fixed dividers is instead used to synthesize the second VCO frequency. Other fixed internal dividers are used to get the comparation frequencies of both loops.

Channel selection is made through the I2CBUS interface , directly from the µP.

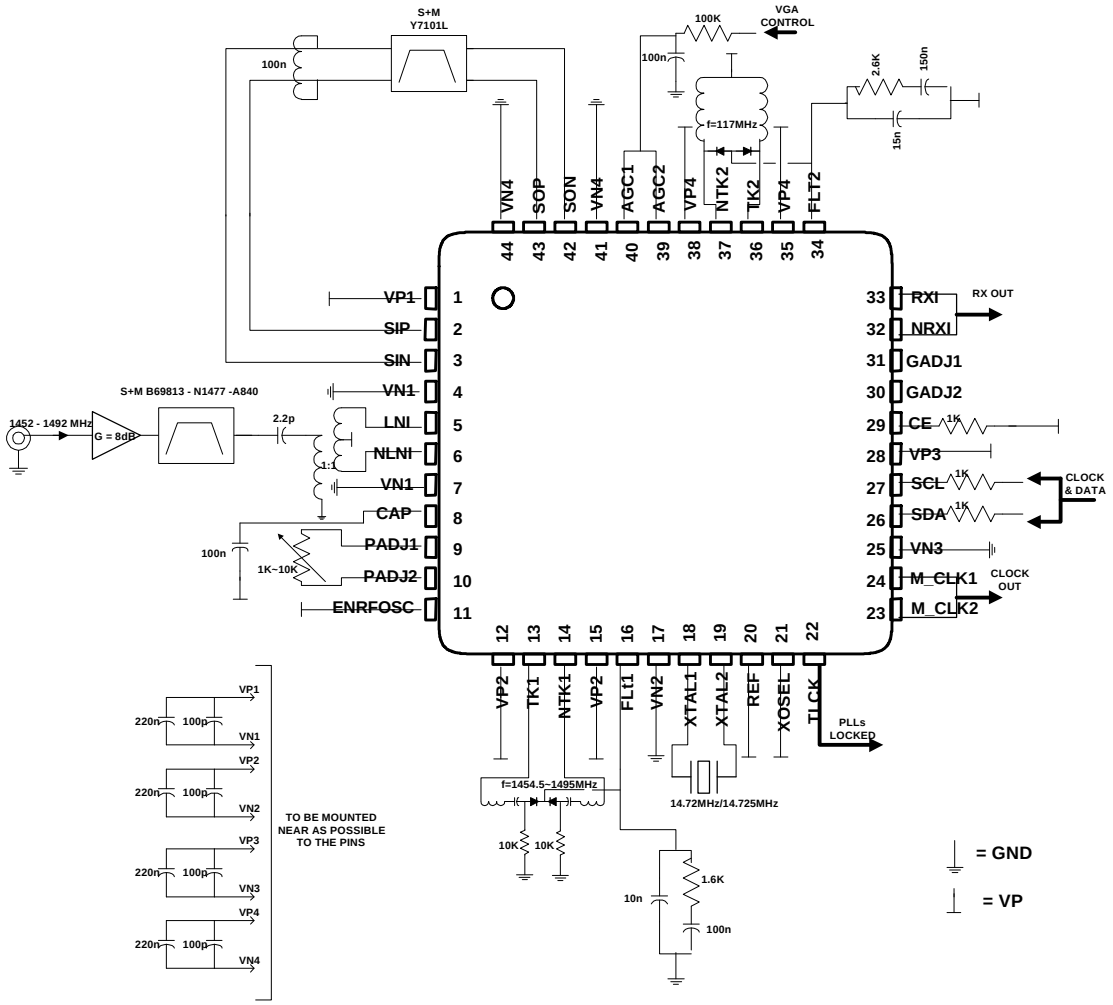
POWER SUPPLIES

The chip operates from an unregulated power supply of 2.7 to 3.3 Volts. All interface circuits to the baseband chips are operated between these supplies unless otherwise specified.

INTERFACE SPECIFICATION

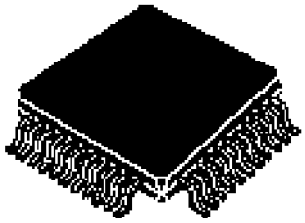
All the interface voltage levels to the micro controller are referenced to the supply voltage of the interface power supply (GND) . The interface voltage levels are therefore fully compatible with base band circuits.
The digital levels are all CMOS threshold compatible with the exception of M_CLK1, M_CLK2 pins (ECL type).
For completeness all other interface signals are also included.

STA001 Application Board Schematic



DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.014	0.018
C	0.09		0.20	0.004		0.008
D		12.00			0.472	
D1		10.00			0.394	
D3		8.00			0.315	
e		0.80			0.031	
E		12.00			0.472	
E1		10.00			0.394	
E3		8.00			0.315	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°(min.), 3.5°(typ.), 7°(max.)					

OUTLINE AND MECHANICAL DATA



TQFP44 (10 x 10)