Espacenet

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Improvements in or relating to electronic digital computing machines

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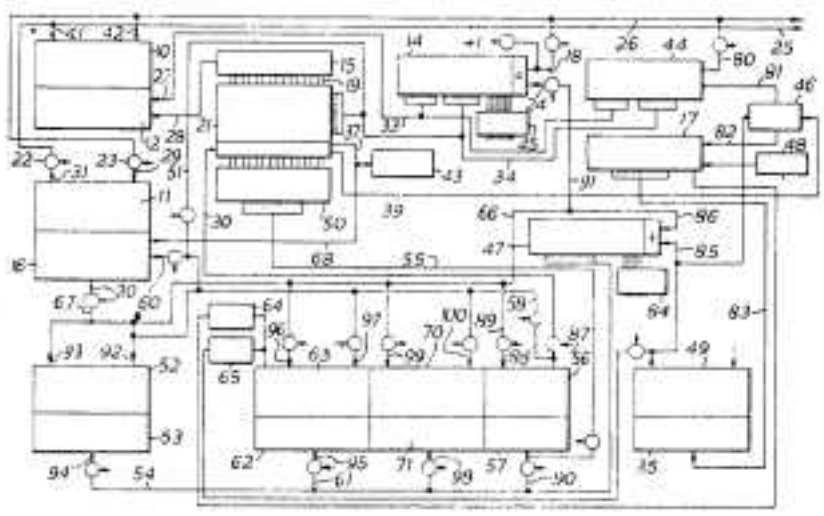
Abstract of GB979632 (A)



979,632. Digital computers. NATIONAL RESEARCH DEVELOPMENT CORPORATION. April 19, 1961 [April 20,1960], No. 13854/62. Headings G4A and G4C. An electronic computing machine includes a high access speed main data store and a secondary data store in which the various storage locations become available sequentially, means being provided to transfer data between the stores, such that each data word is transferred from the main store into that one of the address locations of the secondary store which is unoccupied and next available, a directory register means being provided for recording the programme identification address of each of said transferred data words and the secondary store address to which each of said data words has been transferred. As shown, a parallel-mode computer comprises a main store 10 of eight magnetic core matrices in which words are stored in sixteen blocks of 512 words each and a secondary store 11 comprising at least one magnetic drum each drum having 512 blocks of 512 words in each block. In normal operation, the control number in a control register 44, which may be a counter, applies address selection signals to the selection means 12 of the main store 10, the block identifying part being

fed to a comparator 21 which has sixteen registers set in accordance with the addresses of the blocks actually in store 10, and, assuming that the addressed block is in the store 10, an output on one of sixteen lines 19 causes a code generator 15 to produce a four digit block identifying signal for the selecting means 12, the word identifying signals being fed directly from the register 44 to the input 27. From the address selected in the store 10, the required next instructions is read out to a normal instruction register 14 which then becomes effective to select the required number or data word called for by the instruction. The function digit signals of the instruction in the register 14 are effective via a decoder 45 to produce the required control signals. On completion of the instruction, unity is added or subtracted in the register 44 and the next instruction carried out. If a particular block addressed is not in the main store 10, the comparator 21 produces a signal over a lead 39 to switch 46 to effect automatically a transfer operation by transferring control from the normal control and instruction registers 44,14 to separate transfer control and instruction registers 17,47. The control register 17 is preset to a number which identifies the address within a transfer instruction store 49 of the first transfer sub-routine instruction and transfer instructions are read sequentially from the store 49 to the register 47. A device 50 which may select blocks for clearance in sequence or be arranged to select the least used block, selects the next block number MSC of the store 10 for clearance, the programme block number of its contents being PBT, the programme block number of the required block by PBR, which is assumed located at position SSR of the secondary store 11. Transfer takes place in the following steps: (1) PBR is transferred from the register 14 to a register w1 in a working store 52. (2) The MSC output from the device 50 renders operative a related storage position in a main store block register 56, the contents PBT of which are transferred to a register w2 in the store 52. (3) The output # indicating the next block position available in the store 11 is read to an address w3 in the store 52, this signal # then being read out to modify the transfer instruction register 47 to become effective to address a secondary store directory register 63 which has means to indicate whether the next available block in the store 11 is empty or not. If it is not, # is altered to # + 1 and the process repeated until an "empty" position is found, the empty address being called #E. (4) #E is read out from w3 to modify the transfer instruction register 47 which again selects the relevant address in the secondary store directory 63 and its "empty" indication is altered to "full". (5) PBT from w2 is fed to modify the transfer instruction register 47 to form the address part of an instruction to select, in the programme block directory register 70, that address location which is related to the particular programme block number PBT. The signal #E is then read from address w3 and is written into the selected block position over an input 99. (6) #E is then read from w3 to the address selection means 16 of the store 11 to await this particular block number from the store 11,the arrival of this address allowing transfer of PBT from the main store 10 through a gate 23 to the secondary store 11. On completion of this transfer the signal MSC from the device 50 is applied to select an address in the register 56 into which is written from w1 the record of the new contents of the main store block. (7) PBR is read from w1 to the register 47 to be effective to select in the programme block directory register 70 the block number position SSR in the store 11 of the required block PBR, SSR being read out to w4 in the store 52. (8) SSR is read from w4 to the register 47 which is then effective in the register 63 to alter the SSR indication to "empty". SSR is also effective to address the store 11 and transfer the required block via leads 31,41 to the main store 10. (9) The PBR signal is effective to reset the related bank of triggers in the comparator 21. (10) Control is returned to the normal registers 14, 44. Except during the actual word transfer periods, the main store and control circuits can be used to execute other programmes of lower priority, or other peripheral equipment may be brought into use. The arrangement is also applicable to serial machines. Specifications 976,499 and 979,663 are referred to.