Espacenet

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Improvements in or relating to multiplying arrangements for digital computing and like purposes

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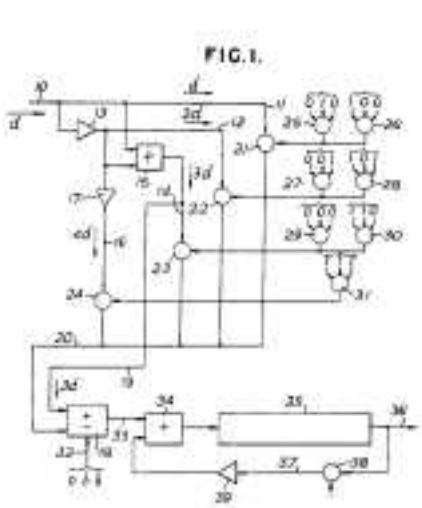
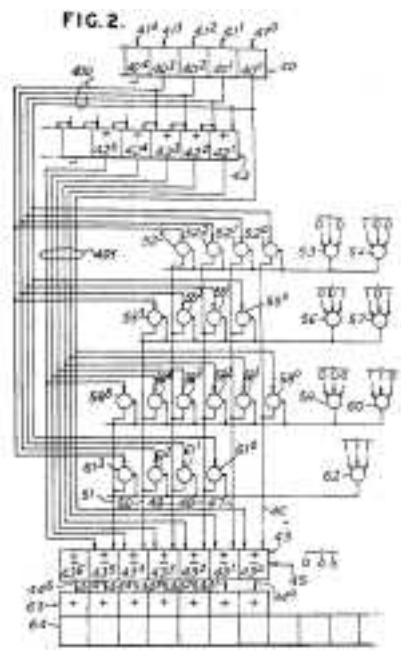
Abstract of GB976620 (A)





976,620. Electric digital multipliers. NATIONAL RESEARCH DEVELOPMENT CORPORATION. March 14, 1961 [March 18, 1960] No. 9720/60. Heading G4A. In a multiplying arrangement of the same general kind as that described in Specification 788,927 in which multiples of the multiplicand are added into an accumulator in accordance with the value of successive groups of digits of the multiplier, means are provided for providing multiples of the multiplicand up to half the total number of multiples capable of being signalled by the chosen number of digits in each multiplier group, appropriate multiples being selected and applied to an adder/subtractor which adds or subtracts them to produce the desired one of the total number of multiples. As described, for serial-mode operation, a multiplicand d is applied to an input 10 to produce, by means of delays 13, 17 and an adder 15, multiples d, 2d, 3d and 4d on lines 11, 12, 14 and 16 respectively. The successive groups of three binary digits of the

multiplier are staticised and control gates 25-31 which in turn control gates 21-24 in the lines 11, 12, 14, 16. The multiple 3d is applied to the "add" input of an adder/subtractor 18 which normally adds, but subtracts if the first of the three digits of a multiplier group is a zero, the subtract input being supplied over a lead 20 with an appropriate multiple d, 2d, 3d or 4d via gates 21-24. The output lead 33 then carries the required partial product of the multiplicand multiplied by a three digit group of the multiplier, which partial product is fed to an accumulator comprising a delay line 35 with feedback via a loop 37. In a modification for parallel-mode multiplication the multiplicand d is registered on flip-flops 40 , 40<SP>1</SP> &c. of a register 40, a second register 42 serving to register 3d. A multi-stage parallel adder/subtractor 43 is controlled over a lead 45 to subtract when the first digit of a group of three multiplier digits is zero. The series of gates 52 -52<SP>3</SP>, 55 -55<SP>3</SP>, 58 -58<SP>3</SP>, 61 -61<SP>3</SP> control the entry of d, 2d, 3d and 4d respectively to the adder/subtractor 43, these gates being controlled by further gates 53, 54, 56, 57, 59, 60, 62 in turn controlled by the multiplier digit groups. The output of the adder/subtractor 43 is fed to an adder and product accumulating shifting register circuit 63, 64. In modifications (Figs. 3 and 4, not shown), the adders 18 or 63 are rendered unnecessary, the circuits for selecting the desired multiplicand multiples being under the control of three multiplier digits and also the examined value of the most significant digit of the previously operative threedigit group.