A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic, and DMOS Power Parts

ANTONIO ANDREINI, CLAUDIO CONTIERO, AND PAOLA GALBIATI

Abstract—**This paper describes a new mixed technology, called Multipower BCD, that, starting from the merging of the VDMOS silicon gate process with the conventional junction isolation process, allows the integration on a single chip of bipolar linear, CMOS logic, and DMOS power functions. The architecture of the process was chosen to optimize the power part, which generally occupies the most chip area. With the DMOS device, many other signal components have been obtained whose electrical and structural characteristics are discussed in relation to some process variables. Many test vehicles have been processed to evaluate the different structures and a first electrical application of the technology is indicated.**

I. Introduction

RAPID ADVANCES in integrated circuit and power technology have created new opportunities to develop integrated circuit families where power and control functions are integrated on the same chip [1]–[5]. To integrate complex systems and subsystems without compromising performance [6]–[8], CMOS devices are the best choice as logic parts because of their high layout density and low power consumption. They also can be utilized for analog functions where very high input impedance is required. Nevertheless, for analog functions bipolar transistors are more suitable because they offer better performances in high gain stages (high transconductance, high output current, and low noise) and in high-precision linear parts (low offset voltage due to high matching in V_{be}).

To put the power in a monolithic system the best way is to use power DMOS devices in place of bipolar power transistors; in fact they exhibit technological compatibility with CMOS silicon gate devices [9], very fast switching speed, no driving power in dc condition, and no secondary breakdown limitation. Thanks to the very high efficiency of power DMOS devices, it is possible to realize chips that deliver very high output powers without high dissipation overcoming the heating effects of high current densities that are the main obstacle to the miniaturization of power switching.

Following these guidelines a new technology called Multipower BCD has been developed. This technology allows the mixing on the same chip of two or more power MOS devices, isolated from each other, which exhibit high-voltage and high-current capability, together with low-level signal and high-voltage components. The first example of this technology mixing bipolar, CMOS, and DMOS devices has been realized in the range of 60 V as the maximum supply voltage for the power part, obtaining at the same time a broad range of breakdown voltages (from 15 to 90 V) for the different signal components.

To evaluate process feasibility, a test chip has been realized that incorporates four integrated n-channel enhancement power DMOS transistors connected in an H-bridge configuration (the power section) and n-p-n, p-n-p bipolar transistors, CMOS, high-voltage p-channel MOS, Zener diodes, junction and polysilicon resistors, and junction and MOS capacitors as signal and passive components. Finally, this technology has been successfully applied to a commercial product, a switch-mode motor driver.

This work describes the development of this new technology. Section II deals with the process architecture and its main key features. In Section III the signal components structure and electrical characteristics are provided. Section IV gives an insight into the design parameters and the electrical features of the DMOS transistors. Finally, Section V covers the applications of this technology, giving some details about the switch-mode motor driver developed by SGS.

II. Device Technology—Process Architecture

The architecture of the Multipower BCD structure is the result of the merging of two well-known technologies: the vertical DMOS silicon gate process and the standard junction isolation technique. The former is the final and winning evolution of the development of a process to obtain power MOS devices; the latter is a well-controlled technique that has been extensively used in integrated bipolar devices and that is less costly to produce compared to the dielectric isolation technique.

The simplest version of this process consists of 10 masking steps: seven from the DMOS process and three from the standard junction isolation technique. With the introduction of some additional masking steps (2 or 3), it is possible to integrate many different structures with minimal disturbance to the basic process.

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The authors are with SGS Microelettronica SpA, Monolithic Microsystem Division, 20019 Settimo Milanese, Milan, Italy.

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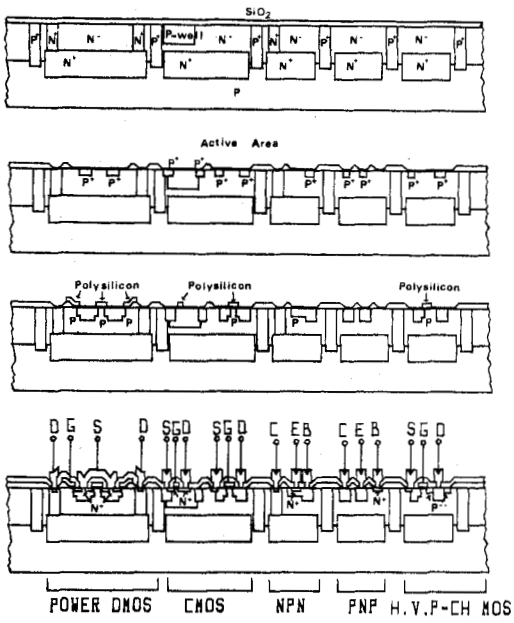

Fig. 1. Cross section illustrating some key processing steps of the 12-mask Multipower BCD process.

The key processing steps, illustrated in Fig. 1, starting from a p-type ⟨100⟩ substrate 2–4 Ω · cm, are:

a) n^+ buried layer antimony implant and diffusion, R_s = 20 Ω/sq.

b) Epitaxial growth of an n-layer 10 μm thick and 1 3 Ω · cm.

c) p-well implant to form the body of the CMOS n-channel FET and the base of a first kind of n-p-n transistor (n-p-n-1), R_s = 5 kΩ/sq.

d) Standard bipolar p^+ isolation and n^+ sinker high-temperature diffusion; after this treatment the p-well junction reaches a depth equal to 4.5 μm (Fig. 1(a)).

e) High-doped p^+ implant to form contact regions, lateral p-n-p emitter and collector, and channel stops in the CMOS n-channel FET.

f) Opening of active areas with tapered oxide steps to improve the performances of the high-voltage devices and step coverage.

g) Gate oxidation (t_{ox} = 850 Å) and boron threshold voltage adjustment implant in CMOS structure without any extra mask.

h) Polycrystalline silicon layer deposition and phosphorus doping.

i) Gates, field plates, and interconnections definition.

j) Boron implant and diffusion (600 Ω/sq) to form the DMOS body, the CMOS p-channel FET source and drain, and the base of other two kinds of n-p-n transistor (a standard n-p-n-2 and an optional n-p-n-3).

k) Drain extension boron implant in high-voltage p-channel MOS transistor without any extra mask (Fig. 1(c)).

l) Heavy arsenic ion implant (R_s = 20 Ω/sq) to form contacts, n-p-n-1 and n-p-n-2 emitters, DMOS source, and CMOS n-channel FET source and drain.

m) After a phosphorus-doped silicon-oxide layer deposition and a gettering step, the whole structure is provided with the conventional next contact opening step, metal deposition, and passivation (Fig. 1(d)).

Adding as an option an extra mask before the gettering step and without modifying the process thermal condition a phosphorus-doped emitter is obtained for the optional n-p-n-3 transistor.

III. Signal Components Structure and Electrical Characteristics

The proposed 12-masking-step mixed technology (13 masks to form optional n-p-n-3) is centered around the vertical DMOS silicon gate process. Using the dopant profiles introduced in the process it is possible to obtain at the same time many different structures with different electrical characteristics.

A. Bipolar Transistors

The electrical characteristics of the lateral p-n-p transistors are connected to the epitaxial layer resistivity and to the spacing between the p^+ junctions of the emitter and collector. In Fig. 2 and in Table I are given the gain behaviors and the more considerable electrical characteristics with regard to four different window spacings of the p^+ diffusions.

In regards to the n-p-n transistors, three kinds of structures are available. The first one (n-p-n-1) is obtained by using as a base the p-well doping profile involved in the CMOS and as an emitter the n^+-As source doping. Its features are: high gain (h_{FE} = 250) and high-voltage capability (BV_{CBO} = 90 V, BV_{CEO} = 40 V, BV_{EBO} = 16 V), but, owing to the high base width (=4 μm), the cut-off frequency is low (=140 MHz).

The second one (n-p-n-2) is obtained by using as a base and as an emitter the same dopant profiles involved in the DMOS transistor to respectively form the body and the source. In this case the gain is low (h_{FE} = 30) but very constant (over more than two decades of I_c current) and very reproducible (spread less than 5 percent) thanks to the controlled characteristics of the process that is essentially a VLSI MOS process. The breakdown voltage capabilities are: BV_{CBO} = 60 V, BV_{CEO} = 35 V, BV_{EBO} = 7.5 V, and the cut-off frequency is about 300 MHz.

With the same base-doping profile of the n-p-n-2 transistor, but with a phosphorus-doped emitter obtained with an extra masking step, it is possible to realize, as an option, the third kind of n-p-n transistor (n-p-n-3). In this case the gain is high (h_{FE} = 200–350) and also the cut-off frequency (f_t = 1 GHz). The n-p-n exhibits BV_{CBO} = 60 V, BV_{CEO} = 25 V, and BV_{EBO} = 7.5 V.

Table II reports the electrical characteristics of the different n-p-n's.

B. CMOS Structures

By adding the p-well diffusion to the DMOS process it is possible to realize self-isolated CMOS structures. The main characteristics of the p- and n-channel MOS in the CMOS structure can be observed in Table III.

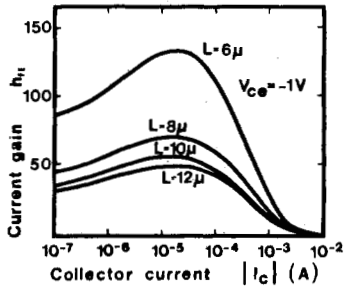

Fig. 2. Current gain versus collector current of p-n-p transistors with regard to four different window spacings L between emitter and collector p^+.

TABLE I
ELECTRICAL CHARACTERISTICS OF LATERAL p-n-p TRANSISTORS WITH DIFFERENT BASE WIDTHS

L (μ)	6	8	10	12
h_{fe}	134	72	57	49
LV_{ceo}(V)	18	45	50	54
BV_{cbo}(V)	62	62	62	62
BV_{ces}(V)	12	62	62	62
BV_{ebo}(V)	75	75	75	75
f_t (MHz)	-	10	-	-

TABLE II
ELECTRICAL CHARACTERISTICS OF THE THREE DIFFERENT KINDS OF n-p-n TRANSISTORS

	NPN1	NPN2	NPN3
h_{fe}	250	27	250
LV_{ceo}(V)	40	40	25
BV_{cbo}(V)	90	64	60
BV_{ebo}(V)	16	7.5	7.5
f_t (MHz)	140	300	1000

TABLE III
MAIN ELECTRICAL CHARACTERISTICS AND GEOMETRICAL PARAMETERS OF DMOS HIGH-VOLTAGE p-CHANNEL MOS AND CMOS

		V_{th}(V)	BV_{dss}(V)	g_m/Z (S/cm) V_{gs}=10V, V_{ds}=5V	$R_{on}\cdot Z$ (Ω·cm) V_{gs}=10V, V_{ds}=0.1V	L_{ch}(μ) (1)	t_{ox}(Å) (2)
CMOS	N-ch	0.9	16	0.161	1.9	3.0	850
CMOS	P-ch	1.9	35	0.073	11.3	2.6	850
P-ch H.V.		1.9	80	0.053	18.0	3.3	850
DMOS		2.7	70	0.25	3.5	1.5	850

$(R_{on}\cdot A)_{Dmos}=(R_{on}\cdot A)_{Si}+(R_{on}\cdot A)_{metal\ layout}=(6+3)\cdot 10^{-3}\ \Omega\cdot cm^2$

(1) mos electrical channel length ; (2) gate oxide thickness

The threshold voltage of the CMOS p-channel FET device is set by the epitaxial layer resistivity whose value is fixed by the breakdown requirement of the high-voltage DMOS device. Its value can be adjusted by an implant of boron ions. The tradeoff between the doping levels of the p-well and the p-channel threshold voltage adjustment gives complementary threshold voltages without inserting any extra masking steps (see Fig. 3). The adjustment is so light that it does not cause any perturbations to the other integrated structures.

As regards the typical latchup susceptibility in CMOS

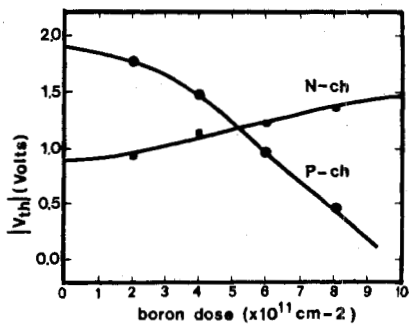

Fig. 3. Threshold voltage of n-channel and p-channel MOS as a function of boron adjustment implant.

TABLE IV
HIGH-VOLTAGE p-CHANNEL MOS BV_{dss} AND $R_{on} \times Z$ VALUES VERSUS DRAIN EXTENSION IMPLANT DOSE

Dose ($x10^{12}cm^{-2}$)	BV_{dss} (V)	$R_{on} \times Z$ (Ω×cm)
2.5	75	32.2
3.0	72	29.8
4.0	91	23.6
5.0	89	17.6
6.0	60	16.0
7.5	46	13.3
9.0	38	11.9
10.0	35	11.2

structures, the combination of an epitaxial layer grown on a low shunt resistance n^+ buried layer and a p^+ ring around the p-well regions gives an improved reliability against this problem up to a maximum operating voltage of 15 V. The current process design rules allow integration of up to 900 MOS transistors per square millimeter.

C. High-Voltage p-MOS Transistor

To satisfy the driving requirements of the high-voltage DMOS device, it is necessary to have a component of inverse polarity sustaining a supply voltage exceeding the DMOS maximum voltage by a value equal to its driving voltage. Adding a boron implant without any extra mask to the 60-V DMOS process it is possible to introduce drain extension regions in a p-channel MOS device increasing its voltage capability up to 80 V. Several process and layout trials have been carried out to optimize the structure. The results are reported in Tables III and IV.

IV. DMOS TRANSISTORS

The power DMOS device consists of a number of transistors with parallel source and gate electrodes integrated on a single isolated area with a common drain. The integration of this component requires bringing the drain contact to the surface via an n^+ buried layer and an n^+ sinker diffusion. The DMOS channel length is very short and does not depend on lithographic accuracy because it is obtained by the difference in lateral diffusion lengths of two different impurity distributions introduced through the same opening in the polysilicon mask. The body lateral

diffusion peak concentration in the channel region sets the threshold voltage of the DMOS device. A heavy-doped p^+ region is formed inside the DMOS body, but outside the channel region, to reduce the value of the pinched resistance under the source that is the base resistance of the parasitic intrinsic bipolar n-p-n transistor. As a consequence the parasitic bipolar latch-back limit increases. In the design of power DMOS components the key parameters are the breakdown voltage, the device ON resistance (R_{on}) for a given area, and the threshold voltage.

A. Breakdown Voltage

To obtain the best tradeoff between maximum (close to ideal) breakdown voltage and minimum epitaxial bulk resistance, design considerations and investigations concentrate on the structure of the edge termination of the p-body/n-epitaxy junctions. In our case an efficient and reliable solution consists in a polysilicon field plate overlaying silicon dioxide of two different increasing thicknesses connected with a very low angle ($\sim 20°$–$30°$), forming a biplanar structure [10]. This edge termination exhibits an efficiency (experimental BV value divided by ideal bulk BV value) of 0.85.

Knowing the edge termination efficiency, the epitaxial layer specification for the Multipower process (60 V) has been established according to minimization of epitaxial layer contribution to the DMOS R_{on}. As a consequence the body–drain junction depletion layer reaches the n^+ buried layer through the epitaxy. The epitaxial layer characteristics are so fixed as follows: $\rho = 1.3\ \Omega \cdot cm$; $W_{epi} = 7.5\ \mu m$.

B. ON Resistance

The R_{on} parameter is strictly dependent on the topological layout that is the shape and size (packing density) of the unit DMOS cell. Besides, the drain electrode positioning on the top adds, with respect to the discrete device, an extra contribution to the R_{on} that depends on the n^+ buried layer drift region, the n^+ sinker contact region, and the layout choice for drain and source interdigitation.

Our goal was to minimize the product $R_{on} \times$ Area, that provides a measure of the efficiency of DMOS design according to a mathematical model.

Studying the structure (DMOS cells) – (n^+ buried layer) – (n^+ sinker) (see Fig. 4), we can give the product $R_{on} \times$ Area as a function of the physical and layout parameters of the component. Using the symbols shown in Fig. 4, we have for the given structure the following expression:

$$R_{on} \cdot \text{Area} = \left\{ \frac{R_c}{N} + \frac{1}{12} \cdot R_{bl} \cdot N + \frac{1}{12} \cdot R_{bl} \cdot \frac{2Y}{l} + \frac{R_{sink}}{l \cdot X_{sink}} \right\} \cdot l \cdot (N \cdot l + X_{sink} + 2Y)$$

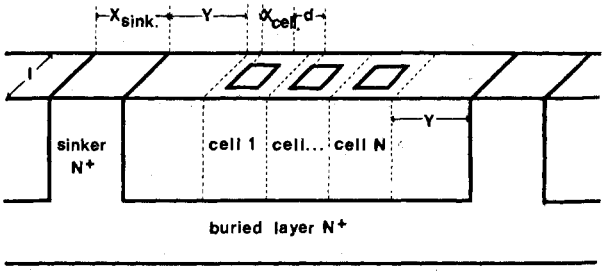

Fig. 4. Model of the integrated power VDMOS for the $R_{on} \times A$ calculation.

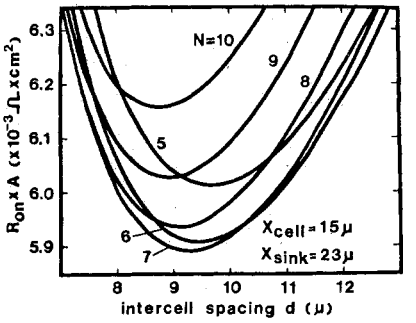

Fig. 5. Theoretical $R_{on} \times A$ as a function of DMOS intercell spacing (d) and number of cells (N) between two drain sinker fingers.

where

- R_c is the ON resistance of the DMOS cell and consists of four distinguishable components,
- R_{ch} is the channel resistance,
- R_{acc} is the accumulation layer resistance,
- R_{JFET} is the parasitic JFET on resistance,
- R_{epi} is the epitaxial layer resistance.

The expression used for R_c relates to the well-known model of the DMOS structure [11], [12].

- R_{bl} is the n^+ buried layer sheet resistance;
- R_{sink} is the n^+ sinker resistance per unit area;
- l is the cell pitch = $X_{cell} + d$, where X_{cell} is the DMOS cell window and d is the spacing between two DMOS cells;
- X_{sink} is the n^+ sinker window width;
- N is the number of cells between two sinker fingers; and
- Y is the distance between the edge of sinker window and half spacing of the last cell (this value includes the extension of the junction edge termination).

According to this model we have written a FORTRAN program that calculates the minimum value for $R_{on} \times$ Area varying the parameters X_{cell}, d, N, and X_{sink}.

As a result of this theoretical calculation, in Fig. 5 the $R_{on} \times$ Area functional dependence on the intercell spacing d, with regard to the different values of the number of cells between the two drain fingers, can be observed. The other two design parameters (X_{cell} and X_{sink}) are considered to be equal to constant values set by additional requirements: $X_{cell} = 15\ \mu m$—as a present technological

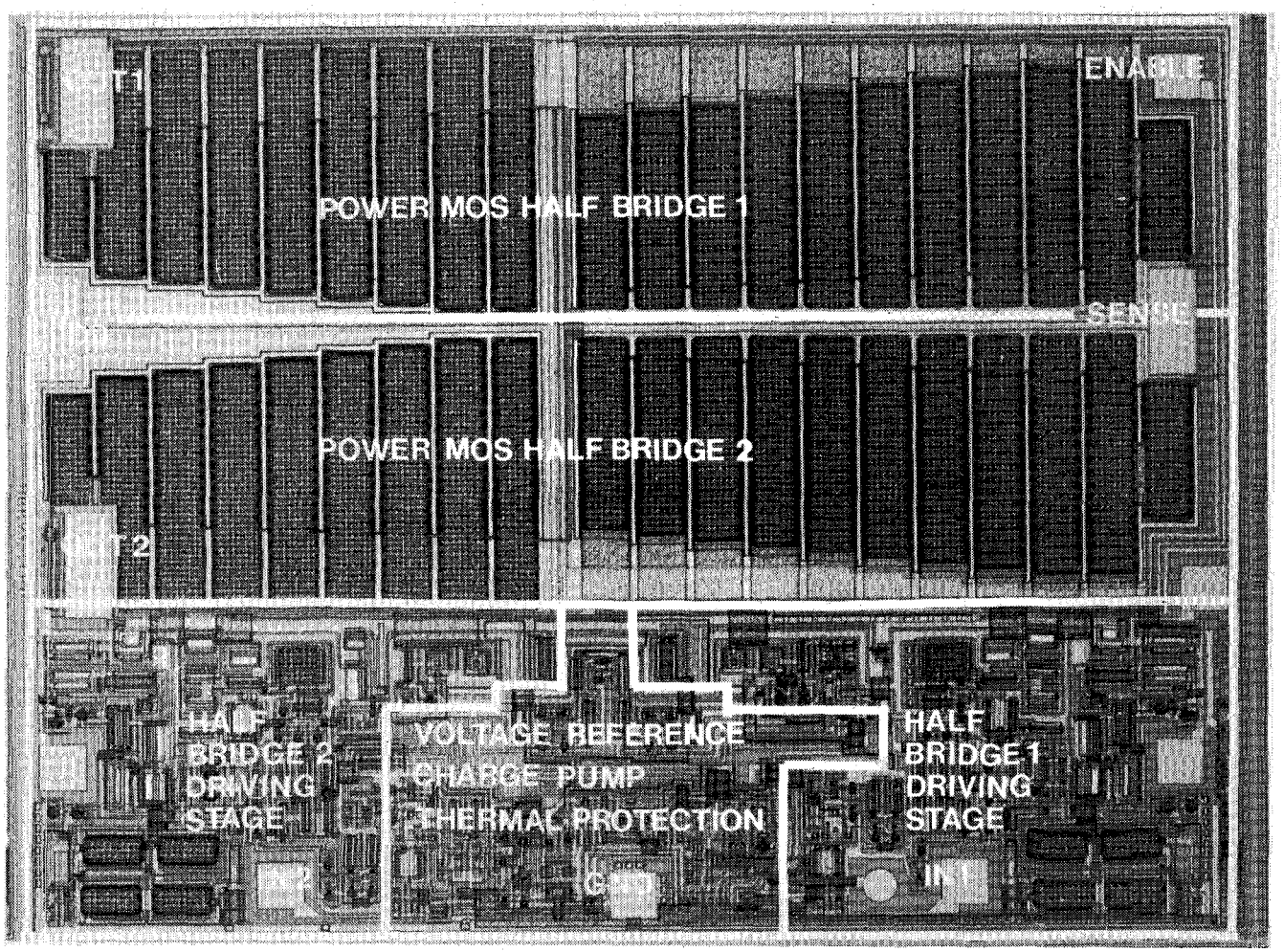

Fig. 6. Photomicrograph of the integrated DMOS H-bridge with the control section.

standard. $X_{sink} = 23$ μm—as imposed by the drain metal strip width needed to lower its contribution to R_{on}.

The minimum value of $R_{on} \times$ Area is found at a value of d in the range from 9 to 10 μm, at $N = 7$ and is equal to 5.92×10^{-3} $\Omega \cdot cm^2$, in good agreement, within 5 percent, with the experimental value (see Table III).

C. Threshold Voltage

The value of the threshold voltage is mainly related to the thickness of the gate oxide and to the peak impurity concentration of the laterally diffused body in the region included between source and drain. The doping profile of the body region is multifunctional in an integrated circuit and consequently many tradeoffs must be satisfied. In fact it is related to the DMOS channel length and to avoid channel punchthrough that could occur under strong reverse bias [13]. Besides, in the Multipower process the body region forms the n-p-n-2 transistor's base, also setting the value of its h_{FE}.

According to these guidelines the tradeoff in Multipower process is:

1) DMOS – channel length = 1.5 μm, $BV_{dss} = 70$ V, $V_{th} = 2.7$ V;
2) n-p-n – $h_{FE} = 25$–30.

Table III summarizes the electrical characteristics of the integrated DMOS transistors.

V. Technology Application

The first product developed with Multipower BCD technology is a full integrated H-bridge control system for dc and stepping motors that can be driven at the input by logic-level TTL or CMOS compatible signals (a chip photo is shown in Fig. 6). This device provides the driving in the switching mode of motors or inductive loads with supply voltages up to 60 V and dc load currents up to 1.5 A and is suitable for operation at high-switching frequencies (300 kHz) and high efficiency [14]. The complete integration of the power stage becomes possible thanks to the free-wheeling diode intrinsic to the DMOS structure that is necessary in applications on inductive loads. In transient conditions the circuit can drive the load with currents up to 5 A for a time limited only by the thermal constant of the package. The level of dissipated power is low (1.5 W at 1.5 A of load current); this feature makes possible the insertion of the die in a cheap DIP package with no need for a heatsink.

VI. Conclusions

It has been shown in this paper that combining the well-known DMOS silicon gate and junction isolation processes it is possible to obtain at the same time a lot of different structures (bipolar, CMOS, DMOS) whose type and characteristics depend on the complexity of the process. The technological approach followed was to center the process around the DMOS silicon gate structure, obtaining the other components adding only two masking steps and two ion implants without any thermal perturbation to the 10-masking-step base process. Our goal was to optimize the power part that generally occupies the most chip area in the main application fields of this technology. The first example of this mixed technology, called Multipower BCD, has been developed in the range of 60 V as maximum rating for the DMOS power part and it was successfully implemented to realize an integrated switched-mode motor driver.

Today the minimum lithographic width employed is 4 μm, but future developments will employ reduced lithographic dimensions and multithickness top metallization, permitting a thin patterned metal over the complex part of the circuit to achieve high packing density and a thick metal over the power section of the monolithic system where there is a need to minimize internal voltage drop.

Future developments will include the realization of processes based on the same concepts but with much higher breakdown voltages (250, 450 V) for off-line applications.

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Antonio Andreini was born in Milan, Italy, in 1957. He received the Laurea degree in physics from the University of Milan in 1983.

For the past two years he has worked at the SGS Microelettronica Central R&D Division on power DMOS discrete devices and has cooperated in the development of power IC's processes based on DMOS technology. In 1985, he joined the Monolithic Microsystem Division R&D Center and is presently working on development of mixed bipolar, CMOS, and DMOS processes.

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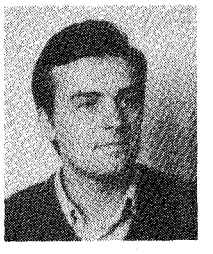

Claudio Contiero was born in Rovigo, Italy, in 1952. He received the Laurea degree in physics from the University of Padua, Italy, in 1976, where he carried on his studies in nuclear physics until 1978.

In the same year, he joined the SGS where he started to develop power MOS processes. In 1982, he joined the SGS Central R&D Laboratory in Agrate Brianza, Italy, where he contributed to the development of the power DMOS process used by the Company's Discrete and Standard Logic Division and to the development of the Multipower BCD process. Since 1985, he has been in the Company's Monolithic Microsystem Division R&D Center, Settimo Milanese, Italy, managing a group developing mixed bipolar, CMOS, and DMOS processes.

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Paola Galbiati was born in Monza, Italy, in 1955. She received the Laurea degree in physics from the University of Milan, Italy, in 1979.

In 1979 she joined SGS Microelettronica, where she conducted her graduate work developing an electrical model on the DMOS device. From 1980 to 1984, she worked in the same field in the SGS Central R&D Division. In 1984, she contributed to the development of mixed bipolar, CMOS, and DMOS processes. In 1985, she joined the Monolithic Microsystem Division R&D Center in Settimo Milanese, Italy.